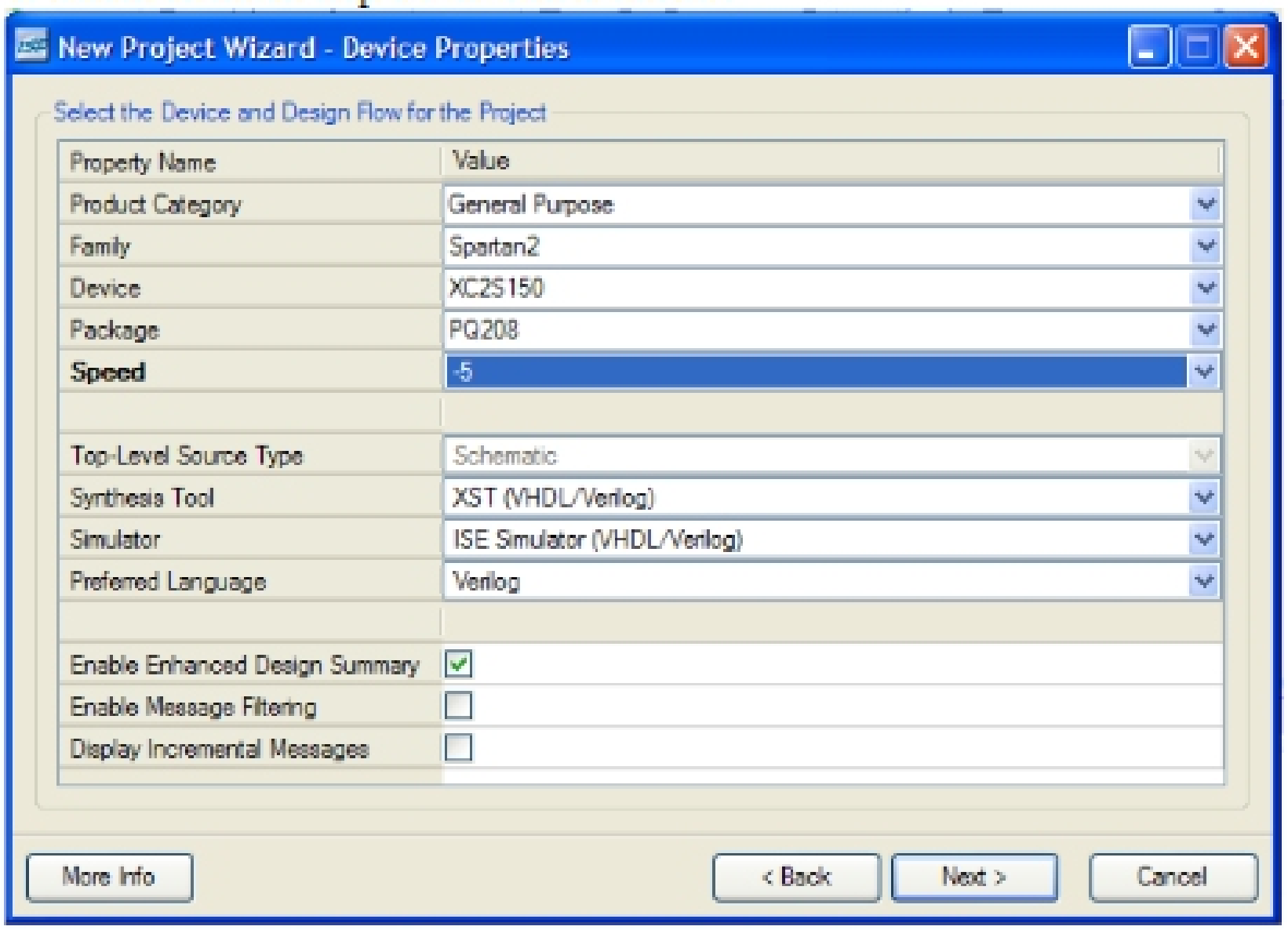
ECT358 – Microprocessors II
Lab 1: Introduction to the Spartan II Development Kit

Objective: To introduce the student to the Spartan II Development Kit and the Xilinx ISE development environment.

Procedures:

1. Open Start-> Programs-> Xilinx ISE -> Project Navigator
2. File-> New Project
3. Give the project a name and location and select top level source type Schematic.
4. Select the device and parameters for our FPGA:



5. Create a new schematic source file by pressing New Source and selecting schematic and naming your file. Make sure that add to project is selected. Select Finish, Next, Next, and finally Finish.
6. There should be 4 windows open: Design Summary, Sources, Processes, and Console. Double click on your schematic file in the Sources window. It should be highlighted in gray underneath the FPGA type. A schematic window will open.
7. To add components to the schematic, click on the add symbol button()
8. To add wires to the schematic, click on the add wire button()
9. To add input and output ports to the schematic, click on the add I/O button()

10. Add the necessary components to the schematic to input the 8 DIP switches and send them to the LED's in order. Additionally, when the pushbutton SW1 is pressed, display the complement of the DIP switches on the LED's.

The ports for the components are as follows:
SW1 P110 SW2 P109 DIP#1 P123 DIP#2 P122 DIP#3 P121 DIP#4 P120
DIP#5 P114 DIP#6 P113 DIP#7 P112 DIP#8 P111 LED D2 P141 LED D3 P140
LED D4 P139 LED D5 P138 LED D6 P136 LED D7 P134 LED D8 P133 LED D9 P132

11. When finished editing the schematic, go to the Sources View of the sources, and the Processes View of the Processes. Inside Design Utilities in the Process View, Right Click on Check Design Rules and select Run. This compiles your schematic.
12. Inside User Constraints assign package pins to the I/O points. A ucf file will be created. In the Location block, enter in the port numbers for the I/O points (P110 for SW1). Save ucf file.
13. Back in the Process View, Right Click on Synthesize and rerun the synthesis.
14. In the Process View, Right Click on Implement Design and select Run.
15. In the Process View, Right Click on Generate Programming File and select Run.
16. Inside Generate Programming File, Right Click on the link that says Generate PROM, ACE, or JTAG file and select Run. This will start the programming software called Impact.
17. A window will pop up that has boundary scan checked. Click on Finish.
18. The software will automatically find two devices, a ROM and a FPGA. Right click on the FPGA and select your .bit file. If the option to program the ROM comes up, click Bypass. Right click on the FPGA and select program. Your FPGA should be programmed now.
19. Verify operation of your program and pass off with the instructor.

Analysis/Conclusions: What can be said of the ease of using the windows interface in programming the FPGA? What did you learn as a result of this lab?