CS 152
Computer Architecture and Engineering

Lecture 21 – Advanced Processors II

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Thanks to Krste Asanovic ..

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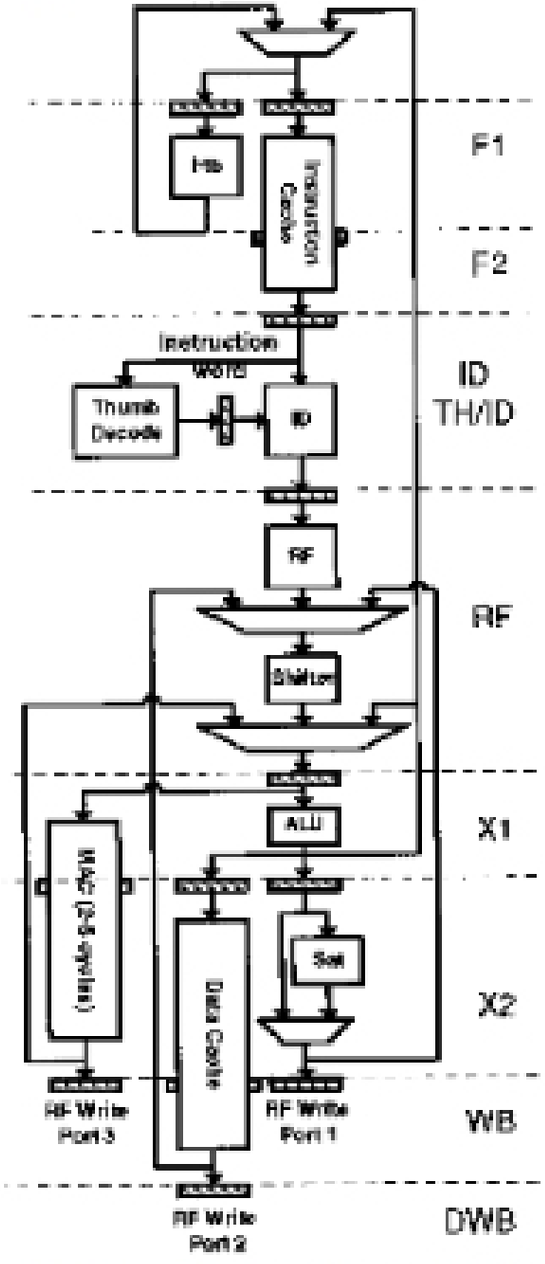
Last Time: Superpipelining & Superscalar



ARM XScale

8 stages

$$\frac{\text{Seconds}}{\text{Program}} = \frac{\text{Instructions}}{\text{Program}} \quad \frac{\text{Cycles}}{\text{Instruction}} \quad \frac{\text{Seconds}}{\text{Cycle}}$$

Q. Could adding pipeline stages reduce CPI for an application?

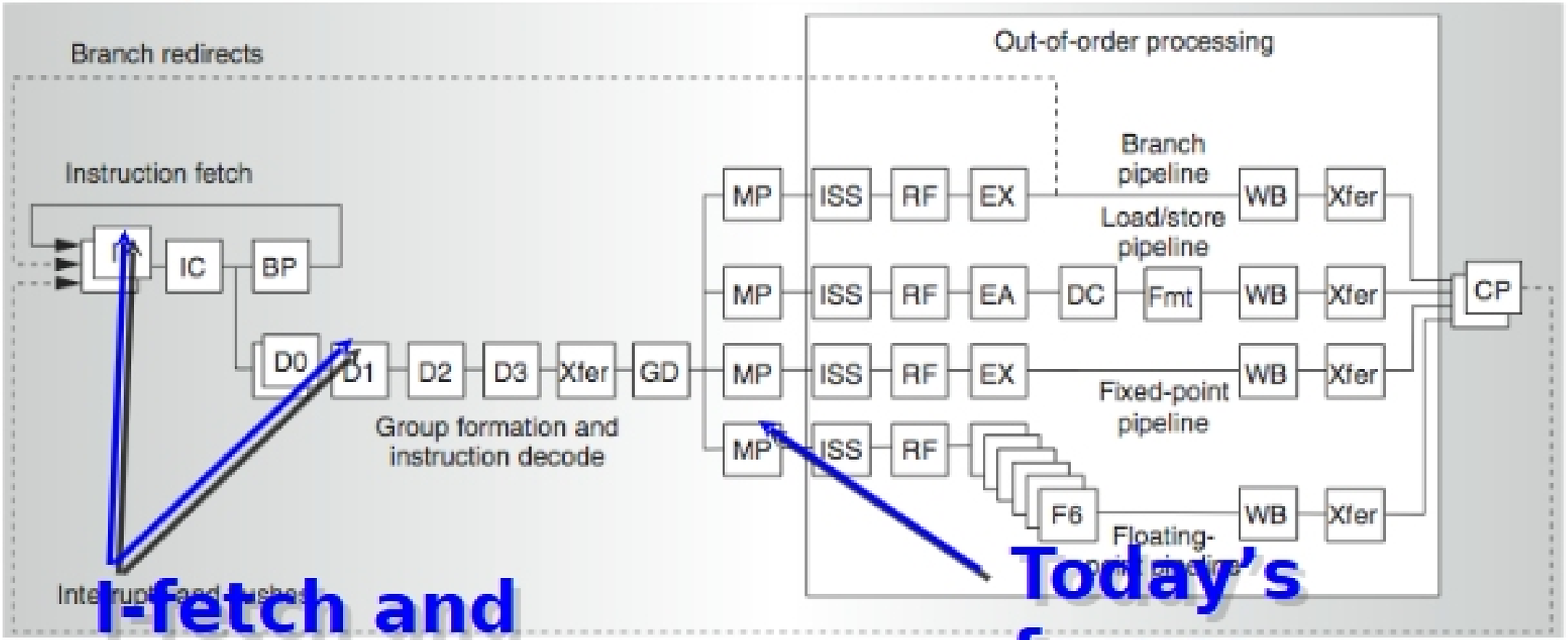
A. Yes, due to these problems:

CPI Problem	Possible Solution
Extra branch delays	Branch prediction
Extra load delays	Optimize code
Structural hazards	Optimize code, add hardware

Today: Dynamic Scheduling Overview

Goal: Enable out-of-order by breaking pipeline in two: fetch and execution.

Example: IBM Power 5:



I-fetch and decode: like static

Today's focus: execution unit