EECS140
Fall 2009
HW3
Due 9/17/09

1)

A. You have a single stage MOS amplifier with a low frequency gain of 100, a pole frequency of 5MHz, and an output capacitance of 1pF. Calculate the unity gain frequency, the transconductance g_m, and the output resistance Ro.
B. You need to design a single-stage amplifier with a gain of 5 at 10^9 rad/sec, and a DC gain of 50. Calculate the unity gain frequency, the pole frequency, and the gain at 10^7 rad/sec and 10^{10} rad/sec.
C. You have a single-stage amplifier with an output resistance of 10^7 Ohms, a transconductance of 10mS, and a unity gain frequency of 10^9 rad/sec. What is the DC gain, the pole frequency, and the output capacitance?

2) Fill in the following table for a single-pole amplifier

	g_m [S]	R_o [Ω]	C_L [F]	Av	ω_p [rad/s]	ω_u [rad/s]
a)	1m	50k	2p			
b)			5p	100	10M	
c)			5p	100		5G
d)		15k			5M	150M
e)		100		5		20G

3) Assuming a common-source amplifier with a PMOS load, for each of the rows above design the amplifier with a bias current and V_{dsat} that gives you the g_m required, while keeping the parallel output resistance of the two FETs greater than Ro, and the total output capacitance less than C_L.

4) For the common source amplifier below, consider channel length modulation in all calculations.

A) Calculate V_{dsatn} and I_{dn} at $V_{out}= V_{dsatn}$ for the NMOS transistor assuming V_{BN} = 0.8 V.

B) Plot I_{dn} vs. V_{out}. What is the minimum and maximum value for I_{dn} which the NMOS device is in saturation in this circuit?

C) What is the value of V_i for which the NMOS device is just on the edge between the saturation and linear regions? (you calculated the current and output voltage at which this happens in part A above). Considering just the current/voltage relationship for the PMOS device, plot $|I_{dp}|$ vs. V_{out} at this V_i on the same plot as step B, and label the curve $V_{i,max}$.

D) What is the value of V_i for which the PMOS device leaves saturation? Again, considering only the PMOS device, plot I_{dp} at this value of V_i on the same plot as B, and label the curve $V_{i,min}$.

E) Based on these values, plot V_{out} vs V_i, paying careful attention to the location of the endpoints of the high gain region (calculated in parts C and D above).

F) Based on the (V_i, V_{out}) pairs that you calculated in C & D, what is the gain of the amplifier in the high-gain region? What are the input and output range over which this gain is achieved?

G) Calculate the gain for this amplifier using the small signal model evaluated at 3 different operating points for V_{out}: the edges of the high gain region, and the center of the high gain region.

H) Use SPICE to make all of the same plots, and comment on any differences between your hand plots and the SPICE plots (there shouldn't be any!). Use spice to plot the gain vs. V_i, and compare to your results in G.