EE 462: Laboratory Assignment 6
Biasing of Transistors: N- channel MOSFET

by
Dr. A.V. Radun and
Dr. K.D. Donohue (10/2/03)
Department of Electrical and Computer Engineering
University of Kentucky
Lexington, KY 40506

Laboratory # 6 Pre-lab due at lab sessions October 14, 15, and 16.
Lab due at lab sessions October 21, 22, and 23.

I. Instructional Objectives

- Analyze the metal oxide semiconductor (MOS) field effect transistor (FET) (MOSFET) using a DC load line
- Design a circuit to set a DC operating point for a MOSFET
- Measure the operating points in a DC biased FET circuit

See Horenstein 5.2, 7.3.1, and 7.3.3

II. Background

Transistors are nonlinear devices, but over certain operating regions they can be approximated with linear models. To ensure a transistor operates in its linear region, a DC level is added to its input signal. The design of this DC level is referred to as biasing the transistor, and the DC values of the transistor's currents and voltages are referred to as the transistor's DC operating point, its bias point, or its quiescent operating point. Once a transistor is biased in its linear region, currents and voltages in a neighborhood around the bias point will vary linearly (approximately). It is assumed that the variation of the transistor's input signal and the transistor's currents and voltages are small enough that they do not move the system into nonlinear regions of operation (triode region or cutoff).

The simplest common source MOSFET amplifier biasing scheme is shown in Fig. 1. Since only the DC operating point is of interest right now, the time varying part of the input signal is omitted. The actual signal would be an AC signal added to the V_{GG} (Gate to Ground DC signal). The transfer characteristic (output as a function of the input) for this circuit can be derived. Apply KVL in Fig. 1 to obtain:

$$V_{out} = V_{DD} - R_D I_D , \quad (1)$$

then using a relationship between I_D and the gate voltage V_{GG} when the MOSFET is in the saturated (forward active) region, Eq. (1) becomes:

$$V_{out} = V_{DD} - R_D \frac{K_p}{2}(V_{GG} - V_{tr})^2 \text{ where } \frac{K_p}{2} = K \text{ (Horrenstein uses } K \text{ and Spice uses } K_p\text{).} \qquad (2)$$

and V_{tr} is the threshold voltage between the cutoff and triode operation region.

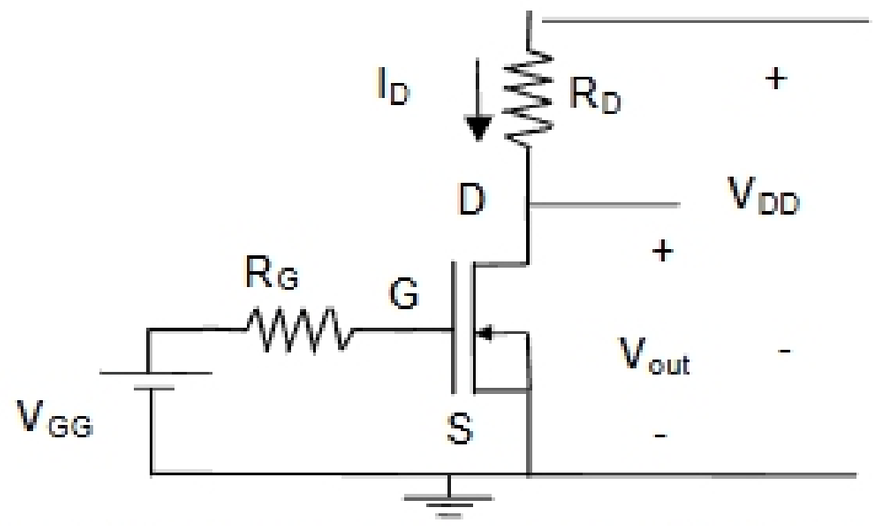

Fig. 1 Basic common source amplifier biasing.

The operating points of V_{GG} and V_{out} are the DC or quiescent values at the input and output, respectively. Ideally, for a given V_{GG}, V_{out} should not vary if the temperature varies or if different transistors of the same type are used. Unfortunately the MOSFET's transconductance parameter K_p cannot be controlled well during manufacturing. In addition, K_p also varies with temperature. For example, the 2N7000 MOSFET transistor's K_p can vary by more than 3.2 to 1. Note that K_p is not directly specified in the data sheet but rather the transconductance gm is specified. The relationship between the MOSFET's transconductance gm and K_p will be addressed in future labs. Since K_p varies significantly, a circuit biased correctly for one transistor may not be biased correctly for another transistor of the same manufacture and part number. Therefore, a more robust biasing scheme than the one shown in Fig. 1 is needed, such that the MOSFET's quiescent operating point is less sensitive to changes in K_p.

Insensitivity of the MOSFET's quiescent operating point can be achieved by adding a resistor R_S into the source branch of the circuit as shown in the Fig. 2. An analysis this new circuit, similar to before, results in the following equations:

$$V_{GG} = V_{GS} + I_D R_S \qquad (3)$$

$$I_D = \frac{K_p}{2}(V_{GS} - V_{tr})^2 = \frac{K_p}{2}(V_{GG} - I_D R_S - V_{tr})^2 =$$

$$\frac{K_p}{2}(V_{GG} - V_{tr})^2 - K_p R_S (V_{GG} - V_{tr}) I_D + \frac{K_p}{2} R_S^2 I_D^2$$

(4)

$$I_D^2 - \left(\frac{2(V_{GG} - V_{tr})}{R_S} + \frac{2}{R_S^2 K_p} \right) I_D + \frac{(V_{GG} - V_{tr})^2}{R_S^2} = 0$$

(5)

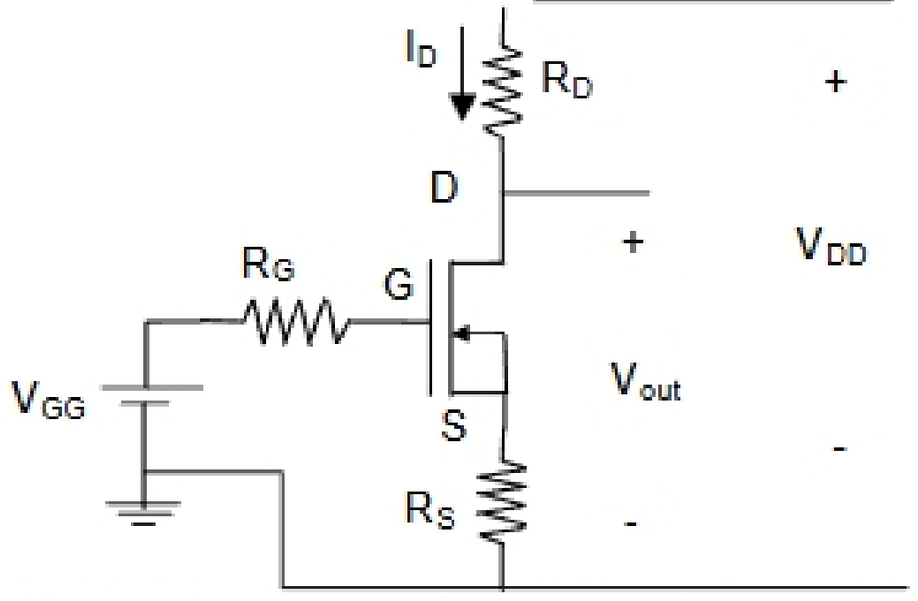

Fig. 2 Basic common source amplifier with reduced K_p sensitivity.

Note that when R_S goes to zero (multiply by R_S^2 and let R_S go to zero), Eq. (5) simplifies to:

$$I_D = \frac{K_p}{2}(V_{GS} - V_{tr})^2$$

(6)

which is the same relationship for the circuit in Fig. 1. (Why should this be expected?) One the other hand, if the R_S is large (relative to 2), then Eq. (5) is approximated by:

$$I_D^2 - \frac{2(V_{GG} - V_{tr})}{R_s} I_D + \frac{(V_{GG} - V_{tr})^2}{R_s^2} = 0$$

(7)

Notice that in Eq. (5), K_p only appeared in one term, whose effect was minimized (relative to the other terms) by a large R_S value. The quadratic in Eq. (7) is a perfect square and can be rewritten as: