A Survey of FPGA Benchmarks

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Abstract

New markets are emerging for the fast growing field-programmable gate array (FPGA) industry. Standard and fair benchmarking practices are necessary to evaluate FPGA systems and determine their potential to support target applications. This paper provides an extensive survey of FPGA benchmarks in both academia and industry.

Keywords: FPGA, Benchmark, Performance, Evaluation, RAW, VPR, MCNC, IWLS, PREP, Toronto 20, LINPACK, DSP, BDTI, MATLAB, MediaBench, OpenFPGA, Smith-Waterman, BLAST, EEMBC, Dhrystone, MiBench, OpenCores.

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1. Introduction

In the recent years, field-programmable gate array (FPGA) systems have gained popularity in many applications such as digital signal processing, high performance computing, biological applications, just to name a few. FPGA, a reconfigurable digital logic device, facilitates rapid prototyping and design verification that enable designers to develop robust hardware and software solutions. A typical FPGA design flow involves: creating an electronic circuit design, placing and routing connectivity of the design onto FPGA architecture, verification and validation of the design, and configuration of the design into an FPGA device [WikipediaFPGA].

The FPGA community relies heavily on benchmarks to evaluate performance of their hardware and software solutions. Therefore, standard and fair benchmarking practices are necessary to evaluate FPGA systems and determine their potential to support target applications. For instance, an end user may study benchmark results published by various FPGA vendors to select an FPGA device that is suitable for the intended application. This survey will explore utilization of benchmarks to evaluate systems that contain FPGA devices and their associated software design tool chains.

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2. Historical Background

The art of benchmarking in FPGA industry is as old as the industry itself. Shortly after FPGA was born in 1984, a benchmark suite consisting of ten combinational benchmark circuits was reported at the International Symposium on Circuits and Systems (ISCAS'85) [Hansen99]. Four years later ISCAS'89 benchmark suite contributed sequential circuits into the FPGA community [Brglez89]. The need for challenging and updated benchmarks led to the introduction of MCNC'91 benchmarks, which were published at the MCNC International Workshop on Logic Synthesis, 1991 [Yang91]. A series of benchmark suites published for conferences and workshops soon followed; they included LGSynth91, HLSynth92, PDWorkshop93, Partitioning93, just to name a few. Microelectronics Center of North Carolina (MCNC), working under ACM/SIGDA grant, maintained free electronic distribution of the aforementioned benchmarks [Brglez93].

Over the years, conference benchmarks have flooded FPGA community because they are more readily available than real industrial benchmarks. Nonetheless, a few non-profit organizations have afforded FPGA industry with benchmarks that span over diverse applications. For instance, PREP'94 benchmark suite was published by a consortium of companies in the programmable logic industry to demonstrate performance and capacity of programmable logic devices [Kliman94]. On the other hand, EEMBC, a non-profit organization formed in 1997 to develop benchmarks for embedded systems [EEMBC08], is an invaluable resource for FPGA system designers implementing soft-core processors. Open-source organizations such as OpenCores allow FPGA community to share real designs, which can be used as benchmarks.

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3. Benchmarks for Traditional FPGA Systems

FPGAs have traditionally been used in reconfigurable and parallel computing systems. Consequently, FPGA community has developed numerous benchmarks to evaluate hardware and software solutions that implement

these systems.

3.1. RAW Benchmark Suite

RAW benchmark suite was published by MIT's reconfigurable architecture workstation project for performance evaluation of reconfigurable computing systems such as FPGA [Babb97]. It implements diverse algorithms in general purpose computing that include CPU and parallel processing benchmarks. Performance of FPGA is based on throughput and resources required to solve a particular benchmark problem. Benchmark results are reported using the following metrics: solution speed (kHz), speedup relative to reference software, and speedup per FPGA [Babb97].

3.2. VPR Benchmark

Versatile place and route (VPR) is a component-level benchmark program contained in SPEC CPU2000 package. It was published by Standard Performance Evaluation Corporation (SPEC) to evaluate compute-intensive integer performance of FPGA during place-and-route design process [SPEC]. VPR demonstrates speed and throughput of performing place-and-route design task. SPEC adopted VPR program from a research project that created it as a tool for packing, placement, and routing designs in FPGA [Betz97]. Although VPR program is not included in the latest SPEC CPU2006 package, it is still popular in the FPGA community.

3.3. MCNC Benchmark suite

Microelectronics Center of North Carolina (MCNC) benchmark suite was published for MCNC International Workshop on Logic Synthesis, 1991. It included logic synthesis and optimization benchmark sets from ISCAS'85 and ISCAS'89 in addition to some other benchmarks collected from industry and academia. The benchmark suite has standardized libraries with representative circuit designs ranging from simple circuits to advanced circuits obtained from industry. MCNC also maintained free electronic distribution of benchmarks originating from past workshops and conferences [Brglez93]. MCNC benchmarks are very popular in academic research. For instance, [Mishchenko06] evaluates runtime performance of their optimization approach using MCNC benchmarks.

3.4. IWLS 2005 Benchmarks

The IWLS 2005 benchmark suite was published by International Workshop on Logic and Synthesis (IWLS). It contains diverse circuit designs derived from past conference benchmarks, open source community of hardware designers, and industry to represent a variety of applications [Albrecht05]. The benchmarks were synthesized and organized into a standardized library with a common timing infrastructure, standard APIs and reporting formats to promote easy exchange of benchmarks and experimental results in the community [Albrecht05]. [Mishchenko06] demonstrates performance of their approach, technique for combinational logic synthesis, by comparing it with runtime of logic synthesis scripts using IWLS benchmarks.

3.5. PREP Benchmark Suite