Batch-Processed Vacuum-Sealed Capacitive Pressure Sensors

Abhijeet V. Chavan, *Senior Member, IEEE*, and Kensall D. Wise, *Fellow, IEEE*

***Abstract*—This paper reports two multitransducer vacuum-sealed capacitive barometric pressure sensors, one using single-lead and the other using multiple-leads to transfer the electrical signal out of the vacuum-sealed reference cavity. The first device operates with a resolution of 37 mtorr over a pressure range from 600 to 800 torr. The sensitivity is 27 fF/torr (3000 ppm/torr). The TCO at 750 torr is 3900 ppm/°C and the TCS is 1000 ppm/°C. The second device has a resolution of 25 mtorr over a range from 500 to 800 torr, with individual transducer sensitivity of 39 fF/torr. The TCO at 750 torr is 1350 ppm/°C and TCS is 1000 ppm/°C. Both devices have an on-chip compensation capacitor and are read out using an electronically-trimmed switched-capacitor charge integrator. [611]**

***Index Terms*—Capacitive sensor, MEMS, pressure, vacuum sealing.**

I. Introduction

WITH an established market of $2.5B [1], pressure sensors are among the most important MEMS devices, with applications in areas such as automotive systems, industrial process control, medical diagnostics, and environmental monitoring (including distributed weather forecasting networks). While a majority of the silicon pressure transducers in use today are piezoresistive, capacitive devices have become the focus for most new developments to achieve higher pressure sensitivity, lower temperature sensitivity, and reduced power consumption. The sensors described here are multitransducer capacitive devices suitable for barometric applications [2]. They have a wide dynamic range (500–800 torr) as well as very high resolution (25 mtorr, equivalent to an altitude difference of about one foot at sea level). These requirements are especially challenging because this resolution must be maintained over a temperature range from $-25\,^{\circ}$C to $85\,^{\circ}$C. To meet this temperature range requirement it is essential that the effects of trapped gas expansion be eliminated [3] through the use of a vacuum-sealed reference cavity. This also results in a device with wider bandwidth by avoiding the damping effects associated with a gas-filled cavity [4]. The first device transfers a single lead (the electrode on the glass) from inside the cavity to the outside world. Parasitic capacitance in parallel with the sensor capacitance has a different thermal behavior than the actual sensing element and thus complicates temperature compensation. The second device has multiple signal transfer leads and significantly reduces such parasitics. During the development of these sensors, specific emphasis was put on making them suitable for planar batch processing and low cost applications. The devices described here are bonded at wafer level and avoid use of glass drilling, epoxy seals, or special metal seals [6], [7].

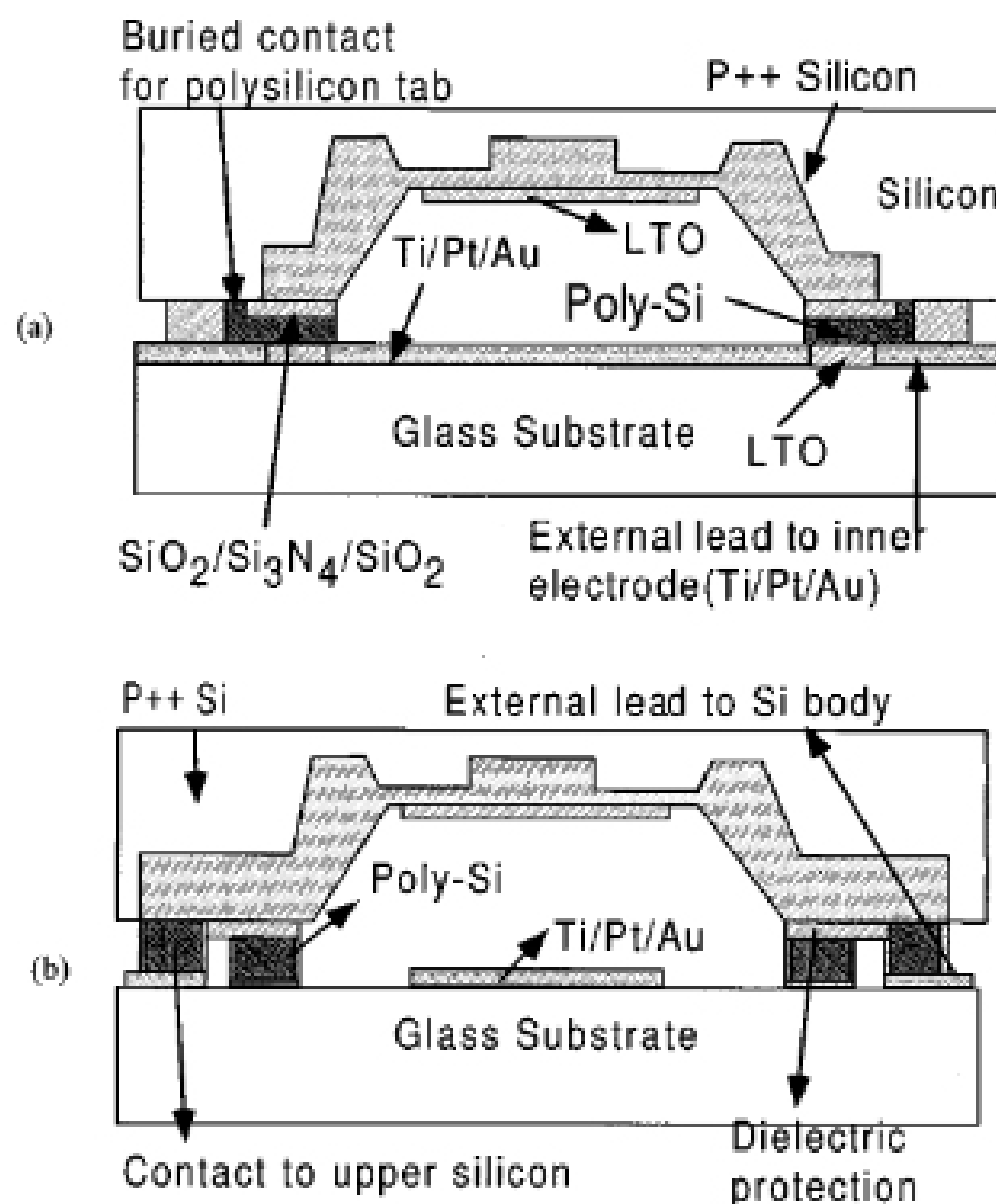

Fig. 1. Cross sections of the capacitive sensor using a single transfer lead from the sealed cavity. (a) The cut is shown through the lead transferring the glass electrode out of the cavity. A tab used to contact the wafer bulk during bonding is also shown. (b) The cut is shown along a device diagonal. The inner ring forms the vacuum seal; the outer ring provides a permanent contact to the silicon electrode.

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A. V. Chavan was with the Engineering Research Center for Wireless Integrated Micro-Systems, Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, MI 48109-2122 USA. He is now with Delphi Microelectronics Center, Delphi Delco Electronic Systems Corporation, Kokomo, IN 46904 USA.

K. D. Wise is with the Engineering Research Center for Wireless Integrated Micro-Systems, Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, MI 48109-2122 USA.

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II. Single-Lead Transfer Sensor

The sensor cross-section is shown in Fig. 1 and consists of vacuum-sealed capacitors realized in a silicon-on-glass dissolved-wafer process. In bringing the glass electrode out from the reference cavity and sealing that cavity in vacuum, one approach is to bring the lead out using polysilicon embedded in a planarizing low temperature oxide (LTO) layer; a second level

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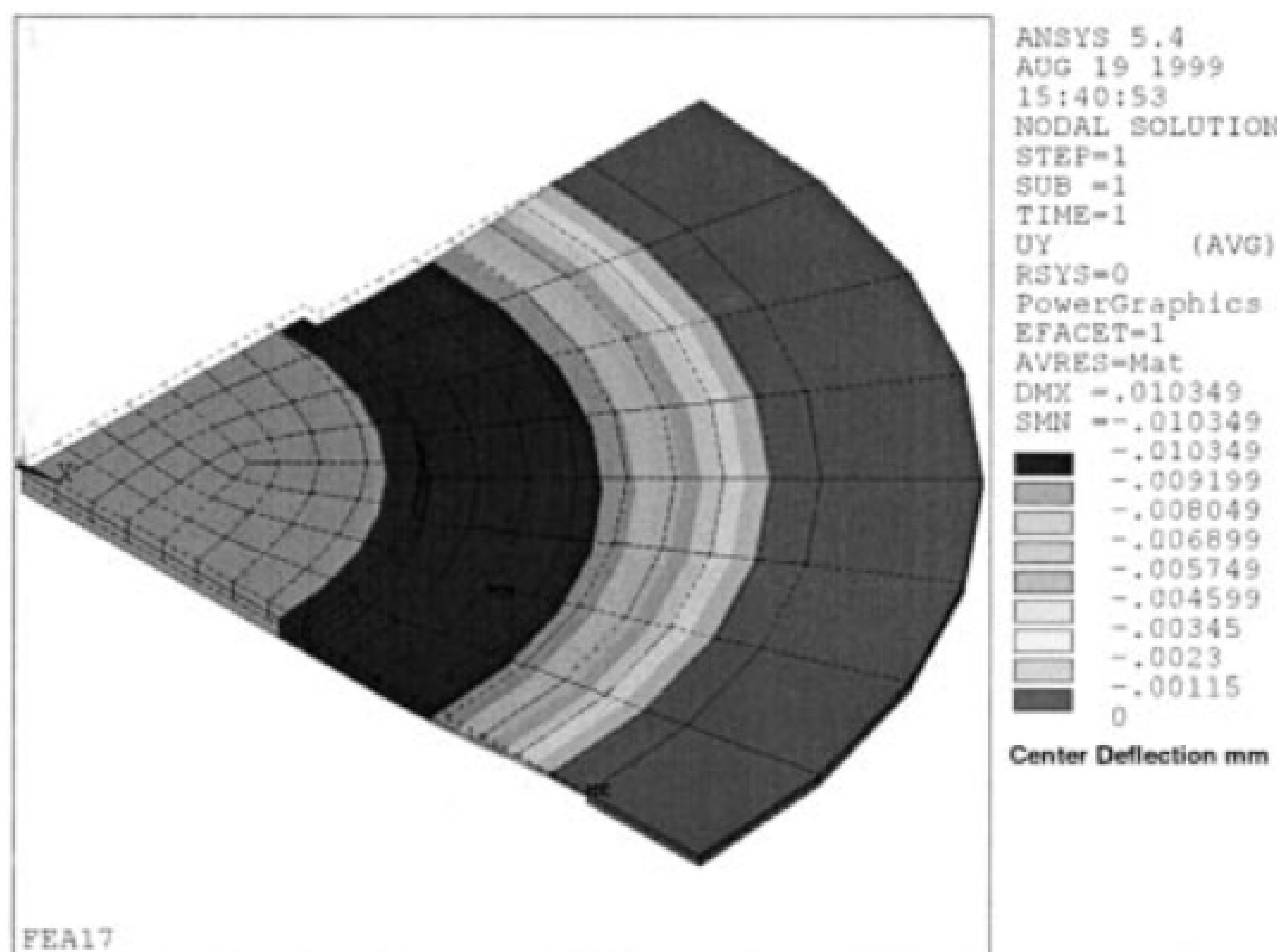

Fig. 2. FEA results for one quarter of a circular bossed diaphragm, showing center deflection for applied atmospheric pressure of 101 kPa.

of polysilicon could then be bonded to the glass substrate. Such seals are known to be hermetic [5]. In the device described here, these two polysilicon layers are collapsed into one layer that functions both as a lead transfer and as a sealing base for the cavity. As shown in Fig. 1(a), the internal sensing lead on the glass is transferred to the polysilicon and then back to metal externally using Pt–Pt bonds formed during the electrostatic bonding operation. Since the polysilicon must be electrically connected to the silicon bulk during bonding but must be well isolated later, lateral polysilicon tabs are used to contact to the lightly-doped portion of the bulk. This area is automatically removed during the etch-back process to provide the required isolation. Permanent contacts to the top silicon electrode are made via similar transfers to the p+ body region as shown in Fig. 1(b). Using this approach, the process flow is much simplified and wafer-level bonds can be made to both 7740 and Hoya SD2 glasses. In addition, since the vacuum seal is done at wafer level before etch-back, the cavity is never exposed to the etch and stiction problems are avoided.

The device has multiple transducers to segment the overall pressure range [2]. The diaphragm diameters vary from 920 to 1100 μm with a gap separation of $\sim$10 μm and a diaphragm thickness of $\sim$3 μm. The device is designed to operate with a resultant diaphragm tensile stress of about 25 MPa. The diaphragm design is done using the ANSYS finite element analysis tool. The center deflection, z, for a circular diaphragm with a rigid center can be obtained to a first order as [16]

$$P = \frac{Et^3}{A_p a^4} y + \frac{B_p E h}{a^4} y^3.$$

Here, P is pressure, E is the Young's modulus, t is diaphragm thickness, a is diaphragm radius, and y is the center deflection. A_p and B_p are constants, which in this case are 0.1135 and 12.4059, respectively. In order to ensure that the diaphragm does not buckle under compressive stress, some residual tensile stress is present in the diaphragm and reduces the center deflection, y. The effect of this residual stress is not accounted for in the equation above. In case of heavily-boron-doped membranes compensated by a thin layer of oxide, this stress is about 25–30 MPa. Fig. 2 gives the finite element analysis (FEA) output, showing the center deflection with all the stress factors present for this diaphragm.

Fig. 3(a) shows a complete five-transducer sensor with an on-chip reference capacitor in the center of the lower row. Fig. 3(b) depicts a single transducer. A scanning electron micrograph (SEM) view of a single transducer is seen in Fig. 3(c).

III. Single-Lead Fabrication Process

A compressed process flow is shown in Fig. 4. The device is fabricated using an eight-mask bulk-micromachined dissolved wafer process. The silicon processing starts with a KOH recess etch of about 9 μm. Small variations in this depth can be compensated in later dielectric deposition steps. A patterned masking oxide [see Fig. 4(b1)] is used to define the anchor area using a solid-source boron diffusion at 1175 °C. A nominal etch-stop depth of 15 μm is obtained. This is followed by a similar masked [Fig. 4(b2)] shallow boron diffusion step to define the diaphragm thickness at about 3 μm. This is followed by 0.08 μm dry thermal oxide grown in O_2 ambient to ensure capping of the boron diffused areas. Next, low-pressure chemical-

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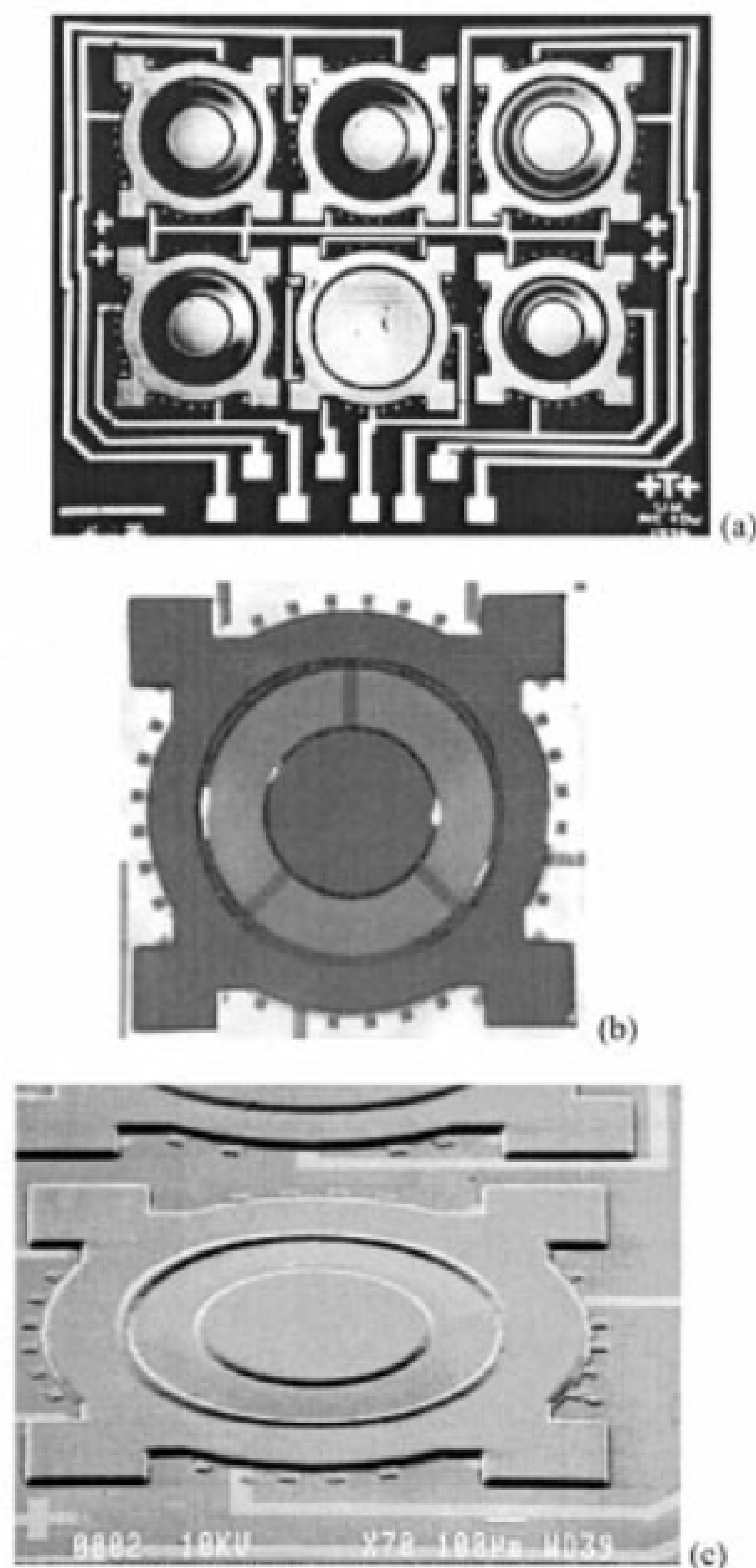

Fig. 3. Top views of the fabricated single-lead-transfer devices. (a) Five transducers are formed per die, having staggered diameters and pressure ranges. A reference capacitor can be seen in the center of the lower row. (b) A back-illuminated view of a single transducer is shown. (c) An SEM picture gives a three-dimensional view of the transducer.

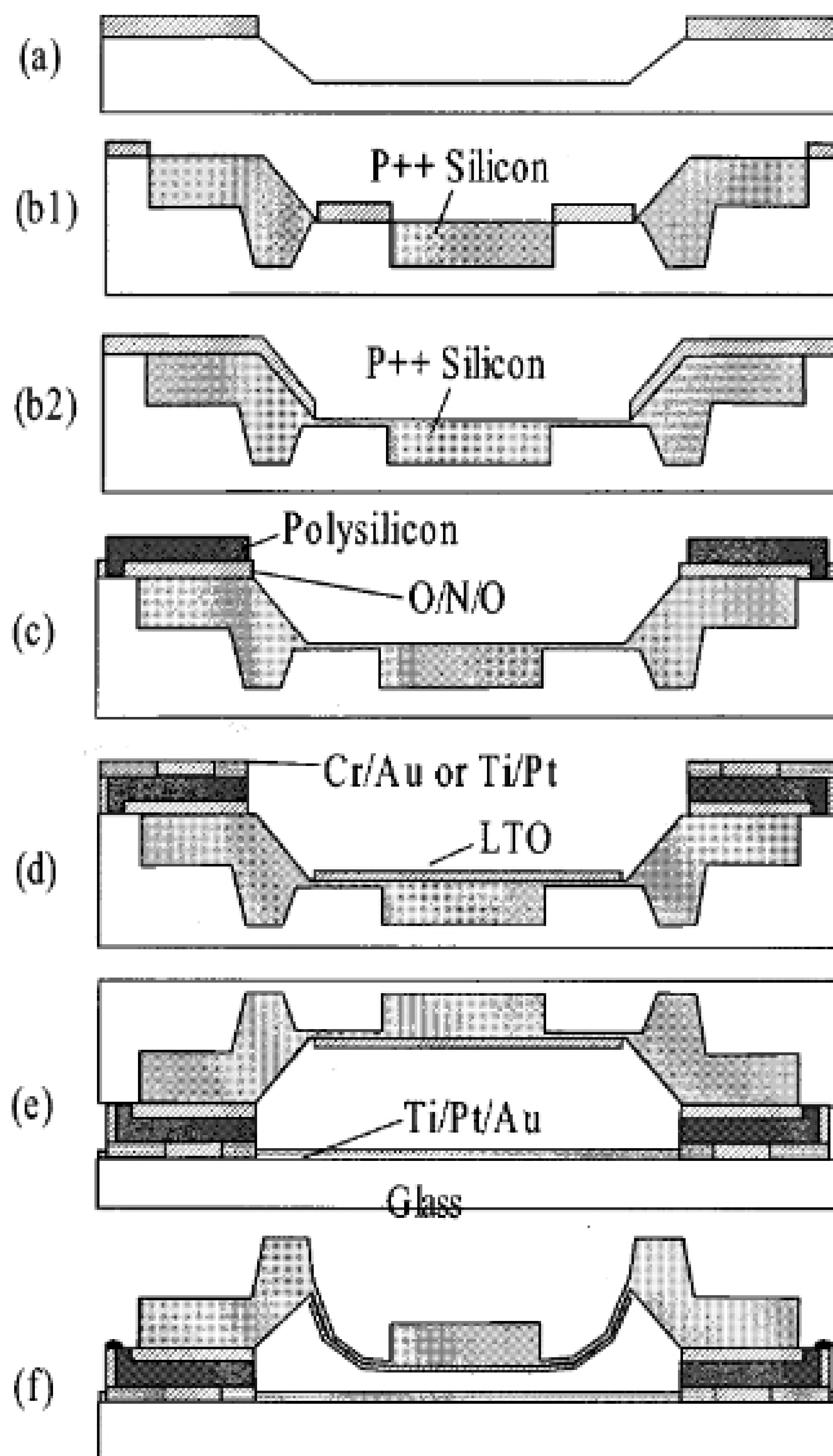

Fig. 4. Process flow for the vacuum-sealed capacitive pressure sensor.

vapor deposition (LPCVD) $SiO_2/Si_3N_4/SiO_2$ dielectrics with thickness of 0.3/0.15/0.3 μm are deposited. Contact openings are patterned to allow the subsequent 1.5 μm-thick polysilicon layer to make contact to the silicon bulk. After depositing the polysilicon, a short boron diffusion at 950 °C is done to reduce the resistance of polysilicon. This also reduces the rate of EDP attack if the protective dielectric coating on polysilicon is broken. Boron diffusion increases the surface roughness of polysilicon to between 80 nm–300 nm. An optional chemical–mechanical polishing (CMP) step can be used to achieve higher yield during vacuum bonding. The use of CMP reduces this roughness below 7 nm and also helps to overcome yield loss due to minor wafer bowing, which may occur in earlier high temperature steps. It is necessary to adopt proper cleaning procedures after CMP [8] to deal with heavy metals from the polishing slurry being embedded in the polished surface. Other options include using *in-situ* doped polysilicon [9], [10] or ion-implantation.

The polysilicon is patterned using an SF_6 plasma. The dielectric layer on the diaphragm area is then removed using wet etching. A 280-nm-thick LTO layer is deposited to protect the polysilicon from attack by EDP. The LTO layer on the diaphragm area also provides isolation for the two electrodes of the capacitor and stress compensation. The LTO layer is patterned to provide for contact openings. Ti–Pt is evaporated with the resist mask for the LTO contact opening still in place, followed by lift-off to provide contacts to the polysilicon with a total height of about 70 nm. This avoids any misalignment between the metal and the LTO contact opening. At this point the polysilicon is completely enclosed in a dielectric layer and has two metal contact areas. Due to the loss of some

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