

University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS150
Fall 2002

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12/6/02

Exam III

Name: _____

ID number: _____

This is a *closed-book, closed-note* exam. No calculators please. You have 2 1/2 hours. Each question is marked with its number of points (one point per expected minute of time).

Put your name and SID on each page. You can work out your answers on the backs of the pages and use the extra blank sheets at the end of the booklet.

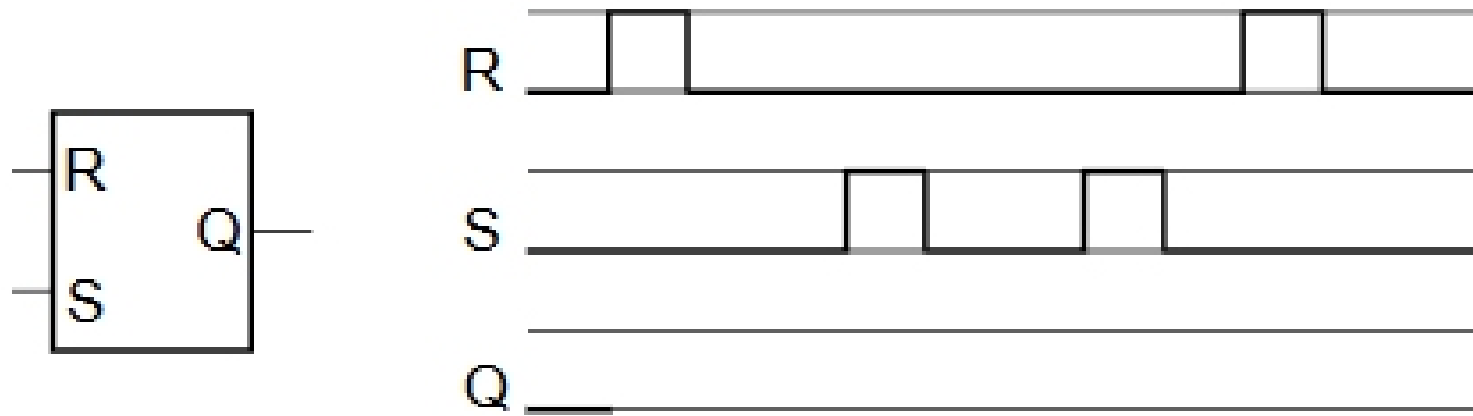
Show your work. Write neatly and be well organized.

Good luck!

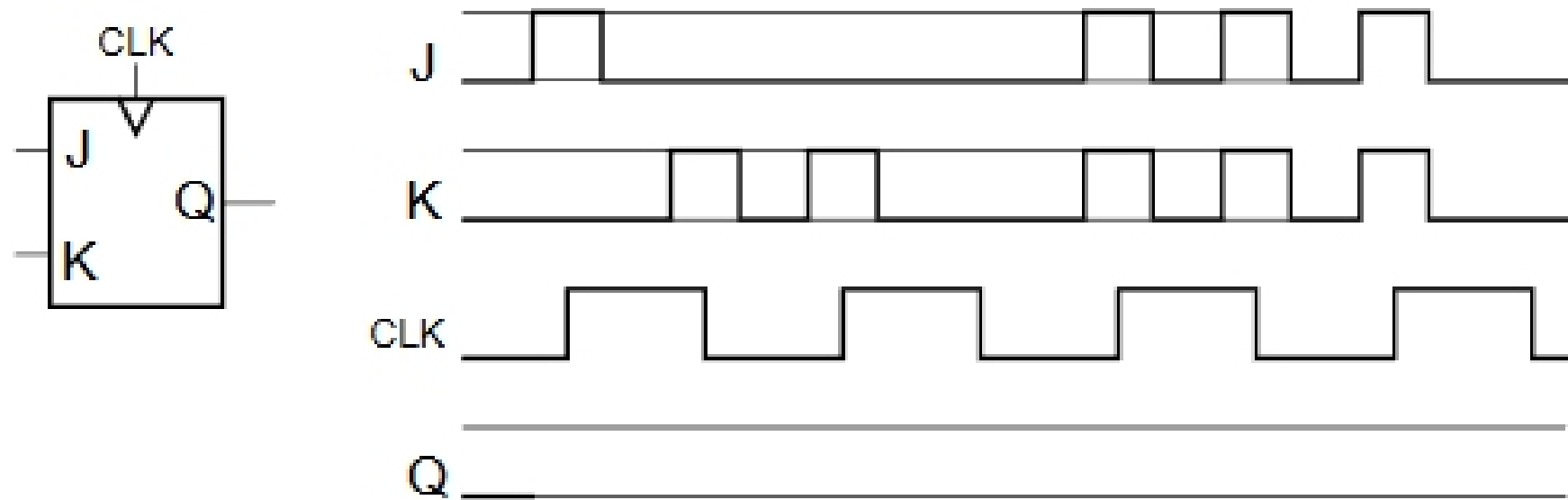
problem	maximum	score
1	10pts	
2	8pts	
3	12pts	
4	12pts	
5	15pts	
6	8pts	
7	10pts	
8	10pts	
total	85pts	

1. [10pt]

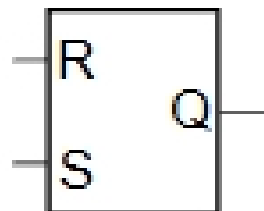
a) Draw in the output waveform for the asynchronous SR latch.



b) Draw in the output waveform for the positive edge-triggered JK flip-flop.



c) Sketch a circuit diagram for a level sensitive D-type latch using only an asynchronous SR latch and simple logic gates:



- d) Sketch a circuit diagram for a positive edge-triggered SR flip-flop using only an asynchronous SR latch, a level sensitive D-type latch, and simple logic gates.