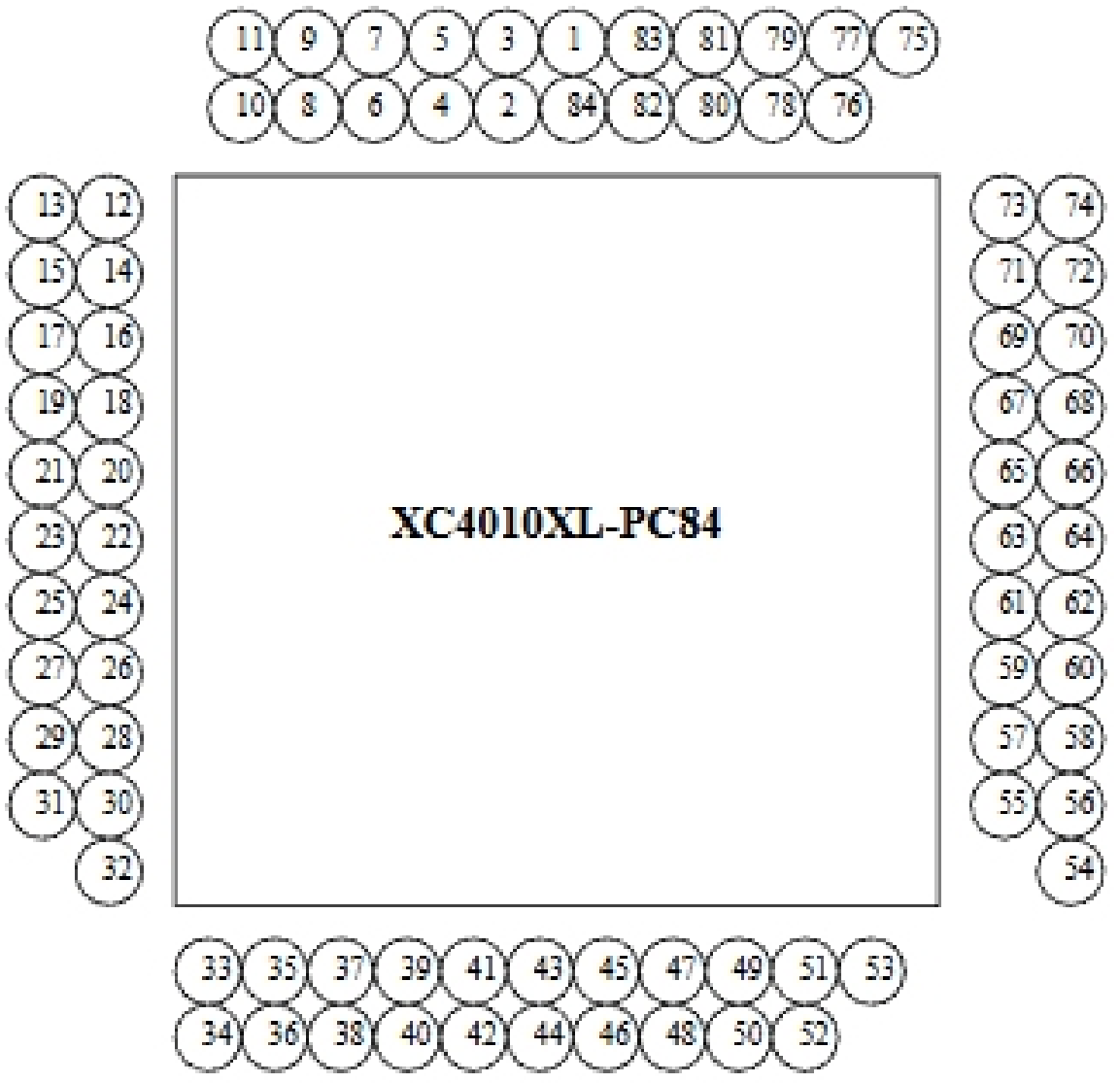
CS150 Fall 2000
Checkpoint 1 Supplementary Material rev1

1) Here is a picture of Xilinx chip pinout on the board.



2) You will need to use 15 and 16 bit busses in this lab so here is some info on bus naming conventions:

For the following example assume XX's are independent wire names or a shorthand for bus name.

A bus name = XX, XX, XX, XX…

Basically one or more XX separated by commas.
A short hand for a bus is the bus names you are used to seeing for example a[7:0].

So "A, B, d[3:4]" is a four bit bus with wires A, B, d3, d4.

You will need to uncheck "simple bus" in the bus naming window to manually enter bus names.

3) Hint for doing FIFO FULL and EMPTY. If you are planning on using adder or subtractor, if you hooked it up right, when the FIFO is EMPTY the output you are looking at should be the same (ie no special cases.), same for FULL. If you want to challenge yourself a bit, you should be able to get the FULL and EMPTY signal with 1 comparator, and a FSM with 1 or 2 bits for state. Also on the handout I said I used 1 adder, 1 comparator, and lots of gates for the FULL EMPTY signal, I actually didn't use a comparator. So not using a comparator doesn't count as a better design than the reference.