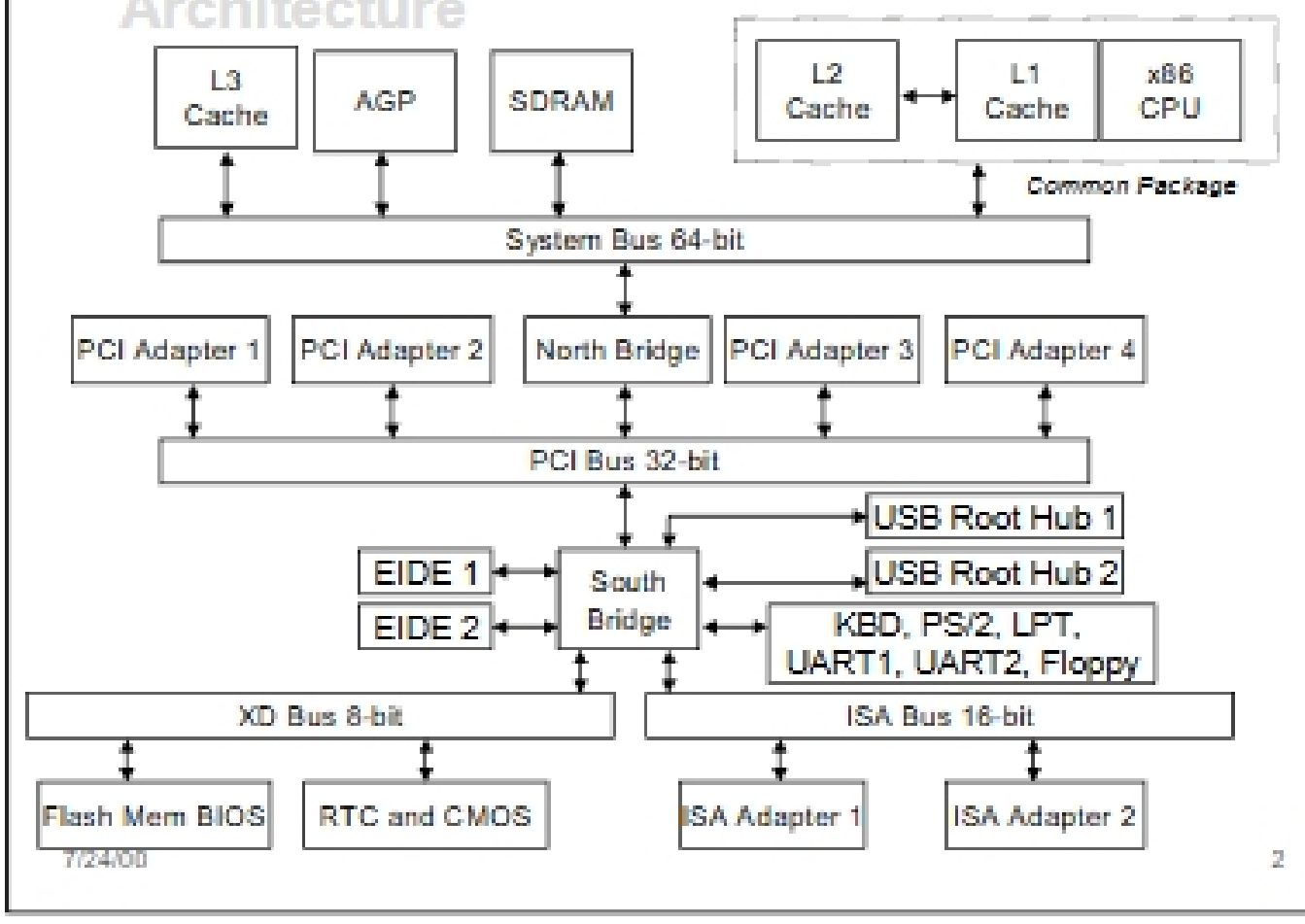
# Motherboard Chipsets

- Provided by CPU manufacturer (Intel, AMD, etc)
- Provide integration of several common functions
  - Cache Controller
  - PCI Bus Interface
  - Dram Controller
  - Bridges to other busses
    - ISA, USB, etc.
- Used to be provided by third party vendors but these could not keep up with complexity of new CPUs, also hard to make time to market goals.

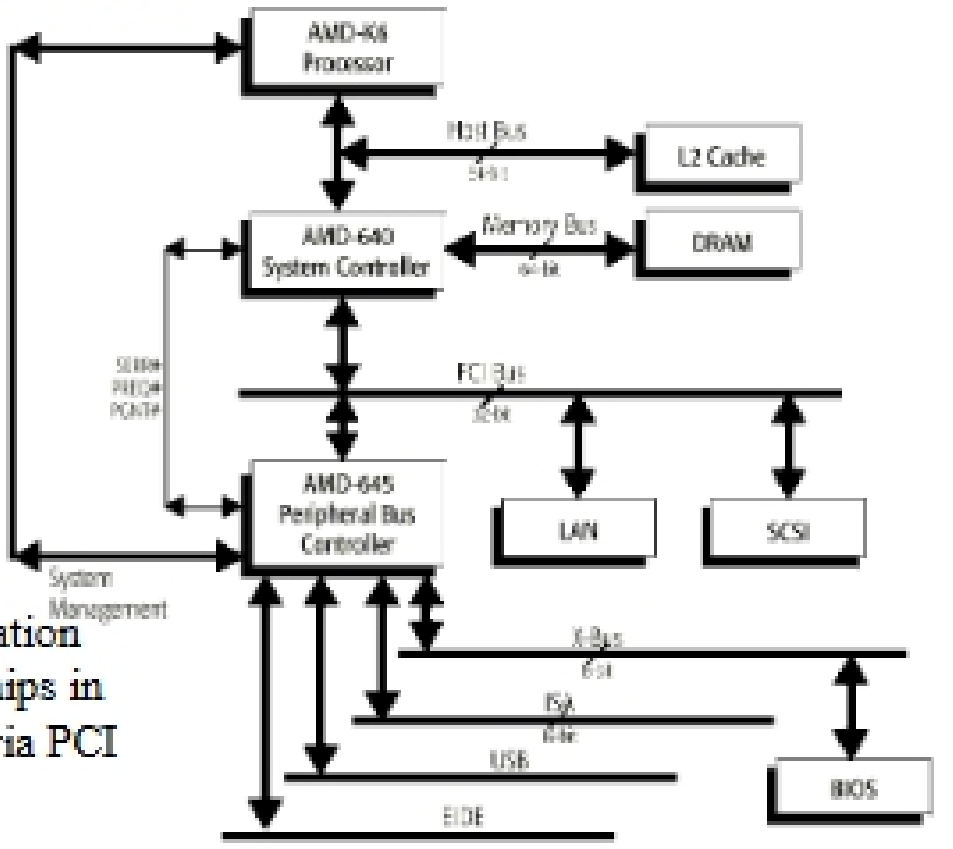
7/24/00 1

## Typical PCI Based x86 Computer Architecture




7/24/00 2

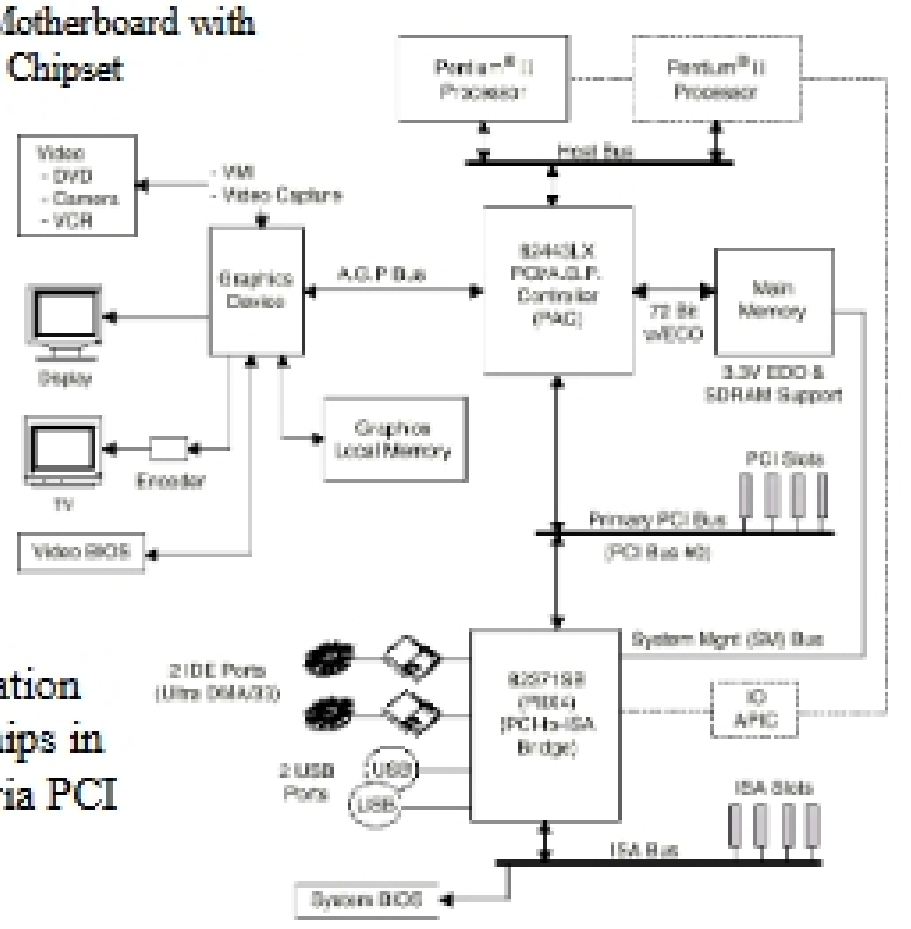
AMD Motherboard




Note that communication between chips in chipset is via PCI bus

7/24/00 3

Pentium II Motherboard with Intel 440LX Chipset

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7/24/00 4

## INTEL 440LX AGPSET: 82443LX PCI A.G.P. CONTROLLER (PAC)

- Supports the Pentium® II Processor at a Bus Frequency of 66 MHz
  - Supports 32-Bit Addressing
  - Optimized In-Order and Request Queue
  - Full Symmetric Multi-Processor (SMP) Protocol for Up to Two Processors
  - Dynamic Deferred Transaction Support
  - GTL+ Compliant Host Bus Supports WC Cycles
- Integrated DRAM Controller
  - EDO (Extended Data Out), and Synchronous DRAM Support
  - Supports a Maximum Memory Size of 512 MB With SDRAM, or 1 GB With EDO
  - 64/72-bit Path to Memory
  - Configurable DRAM Interface
  - Support for Auto Detection of Memory Type: (DIMM Serial Presence Detect)
  - 8 RAS Lines Available
  - Support for +-, 16- and 64-Mbit DRAM devices
  - Support for Symmetrical and Asymmetrical DRAM Addressing
  - Configurable Support for ECC/EC
  - ECC With Single Bit Error Correction and Multiple Bit Error Detection
  - Read-Around Write Support for Host and PCI DRAM Read Accesses
  - Supports 3.3V DRAMs
- Accelerated Graphics Port (A.G.P.) Interface
  - A.G.P. Specification Compliant
  - A.G.P. 66/100 MHz 3.3V Devices Supported
  - Synchronous Coupling to the Host Bus Frequency
- PCI Bus Interface
  - PCI Revision 2.1 Interface Compliant
  - Greater Than 100-MBps Data Streaming for PCI-to-DRAM Accesses
  - Integrated Arbiter With Multi-Transaction PCI Arbitration Acceleration Hooks
  - Five PCI Bus Masters are Supported in Addition to the Host and PCI-to-ISA I/O Bridge
  - Delayed Transaction Support
  - PCI Parity Checking and Generation Support
- Data Buffering For Increased Performance
  - Extensive CPU-to-DRAM, PCI-to-DRAM, and A.G.P.-to-DRAM Write Data Buffering
  - CPU-to-A.G.P., PCI-to-A.G.P., and A.G.P.-to-PCI Data Buffering
  - Write Combining Support for CPU-to-PCI Burst Writes
  - Supports Concurrent Host, PCI, and A.G.P. Transactions to Main Memory
- System Management Mode (SMM) Compliant
- 492 Pin BGA Package

7/24/00 5

## INTEL 820 Chipset (for Pentium III)

82801AA ICH functions and capabilities include:

- PCI Rev 2.2 compliant with support for 33 MHz PCI operations
- Supports up to 6 Req/Gnt pairs (PCI Slots)
- Power Management Logic Support
- Enhanced DMA Controller, Interrupt Controller and Timer Functions
- Integrated IDE controller; Ultra ATA/66
- USB host interface with support for 2 USB ports
- System Management Bus (SMBus) compatible with most $I^2C$ devices
- AC'97 2.1 Compliant Link for Audio and Telephony CODECs
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Alert on LAN*

7/24/00 6