MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science
6.012 Microelectronic Devices and Circuits – Fall 2009

SPECIAL PROBLEM ON CIRCUIT DESIGN – 12/1/09 edition

Issued: Wednesday, November 18, 2009; updated Dec. 1.

Due: Friday, December 4, 2009 and on (be sure that your name is checked off the master list as you hand in your solution). Late solutions will receive zero points; see I.5 below.

Updates: Issues will be dealt with as needed; watch your e-mail.

I. General Comments

Do not panic when you see the circuit. It looks overwhelming at first but it is made up of simple building-block pieces and it is understandable. In addition, you will be given help along the way, first by this write-up, and later in recitations, lectures, and additional handouts. At the same time, the design process you need to go through is a complex one and it is not one you will successfully negotiate in one sitting. Thus it is important that you get started, first developing an understanding of the circuit and the nature of the design challenge, and then at doing your design. You can do it, but not in one night.

II. The Ground Rules

1. Consider this design problem more like an open book exam, than a problem set. You are encouraged to consult references and to seek guidance from the 6.012 staff, and to discuss design issues with others, but you should not work on your specific design and write-up with any other students or any other individuals. Nor should you compare design values or performance results with other students. The design you submit must be your own; any collaborations (and they should be minor) should be noted.

2. Do not let the design slide until the last week. Make a first attempt at a solution early so you can obtain any clarification and guidance you may need from the 6.012 staff before the Thanksgiving holiday (Nov. 26-29).

3. You are required to submit a completed Excel file cover sheet, and a detailed discussion of your design and your approach to arriving at it. The Excel file cover sheet will be available on Stellar. Your write-up should include circuit diagrams for your large signal and incremental analyses, and the equations you used and calculations you made. It should also include a discussion of the trade-offs you considered in your design. View the minimum performance objectives as a challenge and try to do even better.

4. Make reasonable approximations. Do not carry your calculations out to any more than three (3) significant figures. Your predicted performance values should also be stated to no more than three (3) significant figures. The following are examples of numbers with three significant figures: 1.23, 0.123, 123, 3450, 0.0345, 6.78×10^9.

5. Anyone who does not submit a design problem solution which demonstrates a reasonable level of effort will automatically receive zero points and a grade of "I" for 6.012 (as long as their performance is otherwise passing). An "I" received for this reason can only be completed by submitting an acceptable solution to this term's design problem by January 15, 2010. Late solutions will be checked to determine that they are acceptable, but will receive zero points for purposes of determining an overall course grade.

III. Design Objective

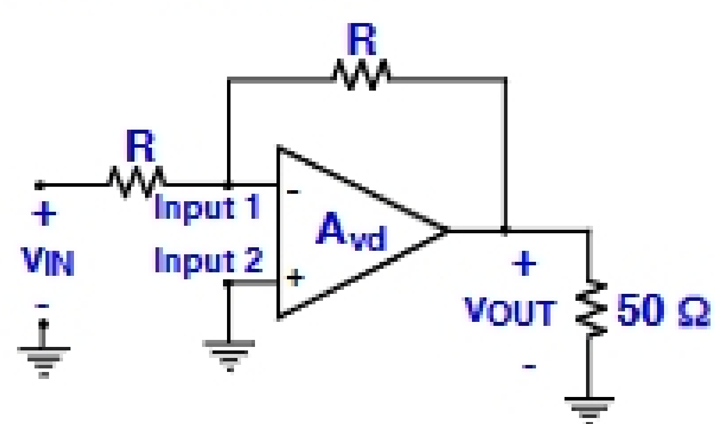
Your design objective is to specify transistor dimensions for the integrated linear amplifier shown in Figure 1 on Page 3 so that it meets or, hopefully, exceeds the performance objectives itemized below. You are able to increase MOSFET gate widths and/or lengths and BJT areas by integer multiples.

The circuit, which is described in full detail in Section V, is a BiCMOS differential amplifier designed to have a large differential-mode gain, large common-mode rejection ratio, large common mode input voltage range, and large output voltage swing.

You are to specify the dimensions of the devices in the circuit in Figure 1, and to calculate the corresponding bias levels and performance characteristics. You are also expected to discuss the main aspects of your design in your solution write-up, and to also discuss there the factors you took into consideration in arriving at your design.

Performance Objectives:

1) Small signal gains defined by writing $v_{out} = A_{vc}(v_{in1}+v_{in2})/2 + A_{vd}(v_{in1}-v_{in2})$
   a) Small-signal differential-mode voltage gain, A_{vd}, into a 50 Ω load: as large as possible, and not less than 125,000
   b) Small-signal common-mode voltage gain, A_{vc}, into a 50 Ω load: as small as possible, and not more than 0.002
2) Common-mode rejection ratio, A_{vd}/A_{vc} : ≥ 5×10^7
3) Small-signal output resistance, r_{out}: ≤ 10 Ω.
4) Maximum output voltage swing into a 50 Ω load, $|v_{OUT}|_{max}$: ≥ 0.75 V.
5) Minimum common-mode input voltage range, $|v_{IC}|_{min}$: ≥ 0.75 V.
6) Total quiescent power dissipation not to exceed 8.5 mW.
7) Output Voltage, i.e. the quiescent voltage at the output, i.e. v_{OUT}, when $v_{IN} = 0$, in a feedback circuit like that illustrated to the right assuming perfect element matching: $|V_{OUT}| \le 20\ \mu V$.



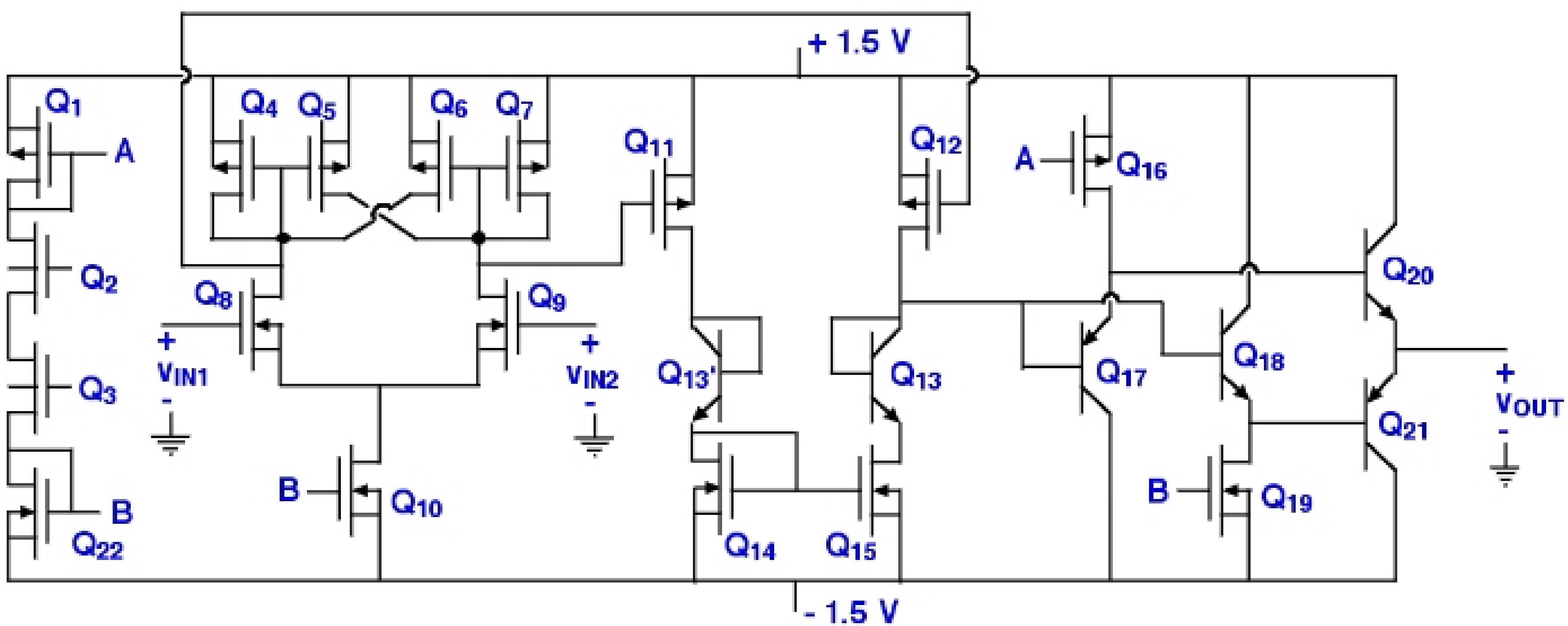


Figure 1 - The Fall 2009 Design Problem circuit, a high gain BICMOS differential amplifier with enhanced common-mode rejection ratio.