6.012 - Microelectronic Devices and Circuits

Lecture 15 - Digital Circuits: CMOS - Outline

- **Announcements**
  - One supplemental reading on Stellar
  - Exam 2 - Thursday night, Nov. 5, 7:30-9:30
- **Review - Inverter performance metrics**
  - **Transfer characteristic:** logic levels and noise margins
  - **Power:** $P_{ave,\ static} + P_{ave,\ dynamic}$ $(= I_{ON} V_{DD}/2 + f\, C_L V_{DD}^{\ 2})$
  - **Switching speed:** charge thru pull-up, discharge thru pull-down
    - **If can model load as linear C:** $dv_{OUT}/dt = i_{CH}(v_{OUT})/C_L$; $= i_{DCH}(v_{OUT})/C_L$
    - **If can say i_{CH}, i_{DCH} constant:** $\tau_{HI\text{-}LO} = C_L(V_{HI}-V_{LO})/I_{CH}$; $\tau_{HI\text{-}LO} = C_L(V_{HI}-V_{LO})/I_{DCH}$ (often only 10 to 90% swings)
  - **Fan-out, fan-in**
  - **Manufacturability**
- **CMOS**
  - Transfer characteristic
  - Gate delay expressions
  - Power and speed-power product
- **Velocity Saturation**
  - General comments
  - Impact on MOSFET and Inverter Characteristics

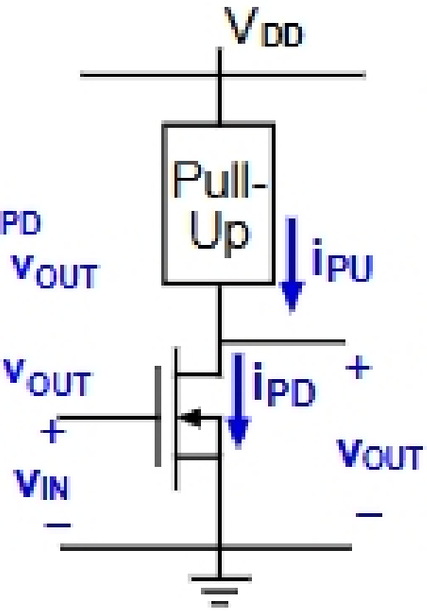
Transfer characteristic

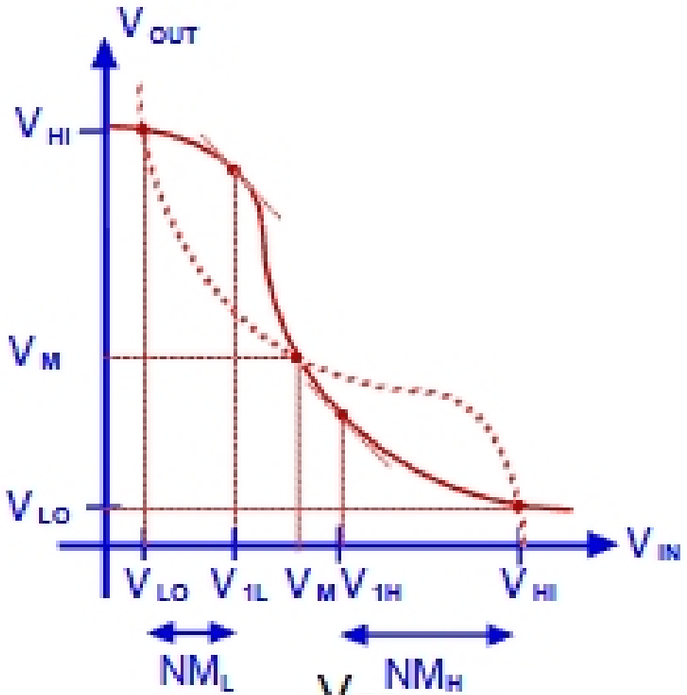
Node equation: $i_{PD} = i_{PU}$

$$i_{PD} = \begin{cases} 0 & \text{for } v_{IN} < V_{T,PD} \\ K_{PD}(v_{IN}-V_{T,PD})^2/2 & \text{for } v_{IN}-V_{T,PD} < v_{OUT} \\ K_{PD}(v_{IN}-V_{T,PD}-v_{OUT}/2)\,v_{OUT} & \text{for } v_{IN}-V_{T,PD} > v_{OUT} \end{cases}$$

i_{PU}: Depends on the device used

Gives us: V_{HI} **and** V_{LO}
NM_L **and** NM_H





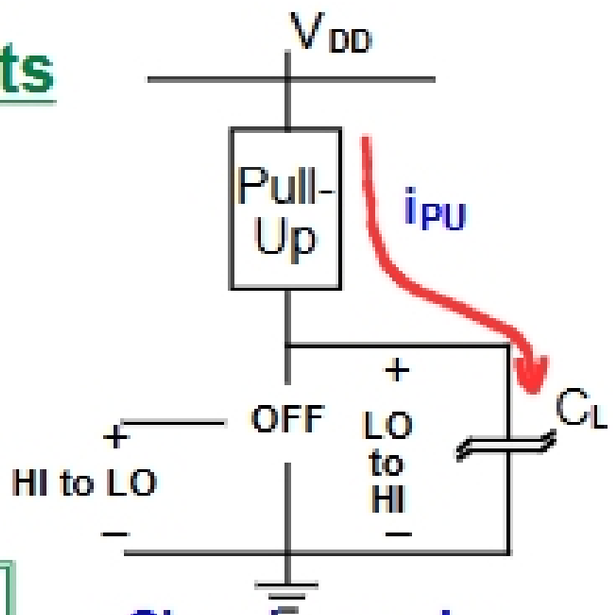
Switching transients

General approach:

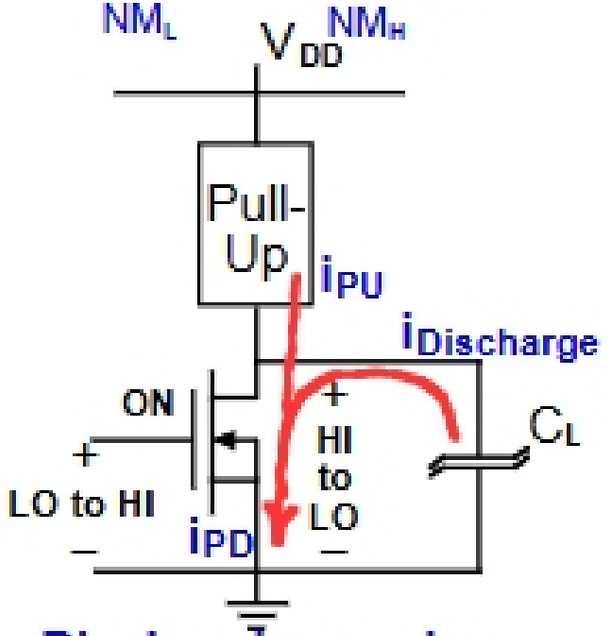
The load, C_L, is a non-linear charge store, but for MOSFETs it is fairly linear and it is useful to think linear:

$$dv_{out}/dt \approx i_{CL}/C_L$$

Bigger current → faster v_{OUT} change



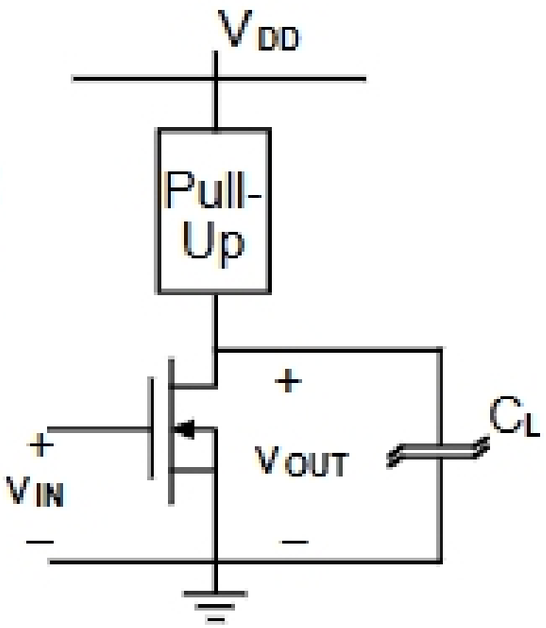
Charging cycle:
$i_{Charge} = i_{PU}$



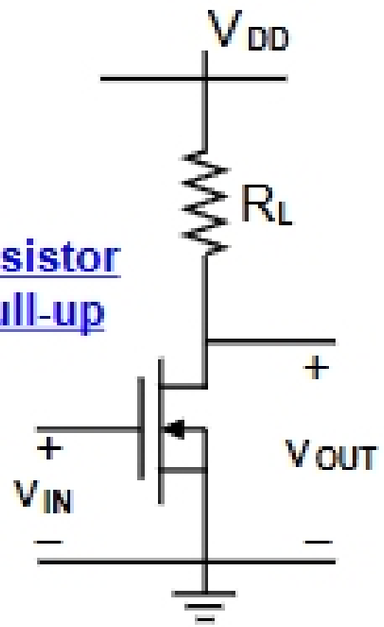
Discharging cycle:
$i_{Discharge} = i_{PD} - i_{PU}$

MOS inverters:

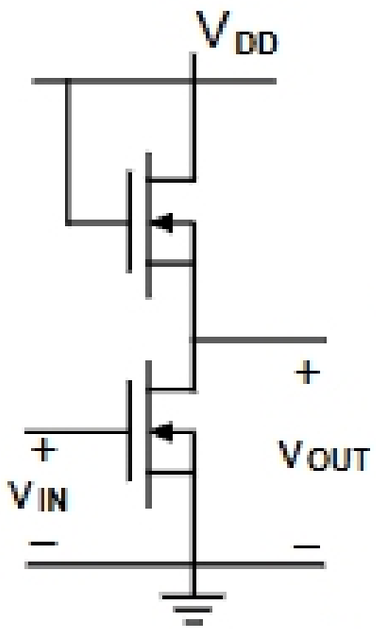
5 pull-up choices

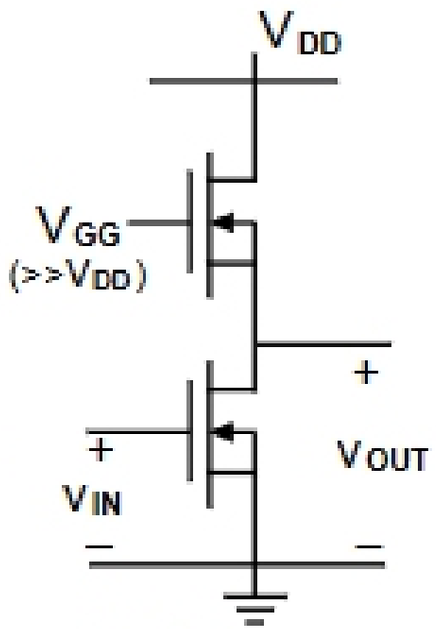


Generic inverter



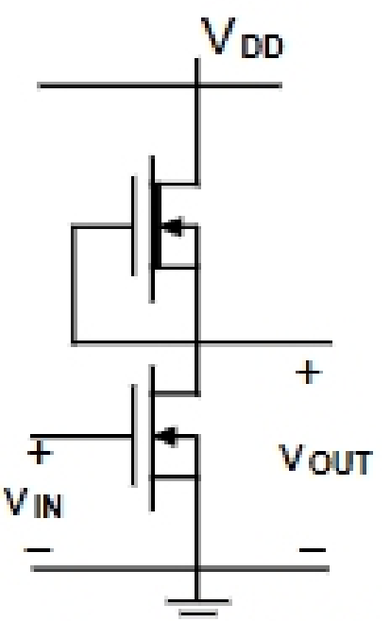
Resistor pull-up



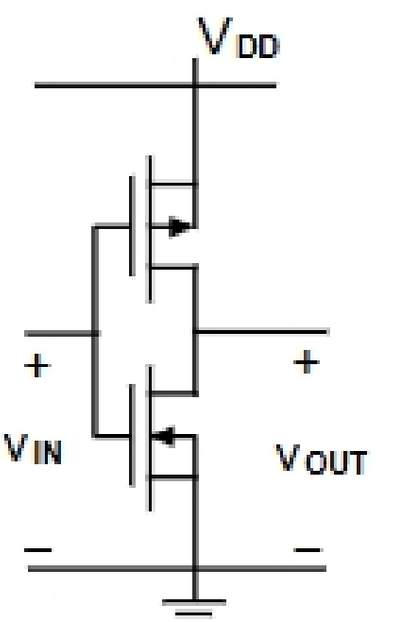


n-channel, e-mode pull-up

V_{DD} on gate V_{GG} on gate



n-channel, d-mode pull-up (NMOS)



Active p-channel pull-up (CMOS)**

* Known as PMOS when made with p-channel. ** Notice that CMOS has a larger (~3x) input capacitance.