CS 152 Computer Architecture and Engineering

Lecture 12 - Complex Pipelines

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Last time in Lecture 11

- Modern page-based virtual memory systems provide:
  - Translation, Protection, Virtual memory, to allow main memory to act as a cache of a larger disk memory, equivalent
- Translation and protection information stored in page tables, held in main memory
- Translation and protection information cached in "translation lookaside buffer" (TLB) to provide single cycle translation+protection check in common case
- VM interacts with cache design
  - Physical cache tags require address translation before tag lookup, or use untranslated offset bits to index cache
  - Virtual tags do not require translation before cache hit/miss determination, but need to be flushed or extended with ASID to cope with context swaps. Also, must deal with virtual address aliases (usually by disallowing copies in cache)

Complex Pipelining: Motivation

Pipelining becomes complex when we want high performance in the presence of

- Long latency or partially pipelined floating-point units
- Multiple arithmetic and memory units
- Memory systems with variable access time