

# CS152 – Computer Architecture and Engineering

## Lecture 15 – Virtual Memory

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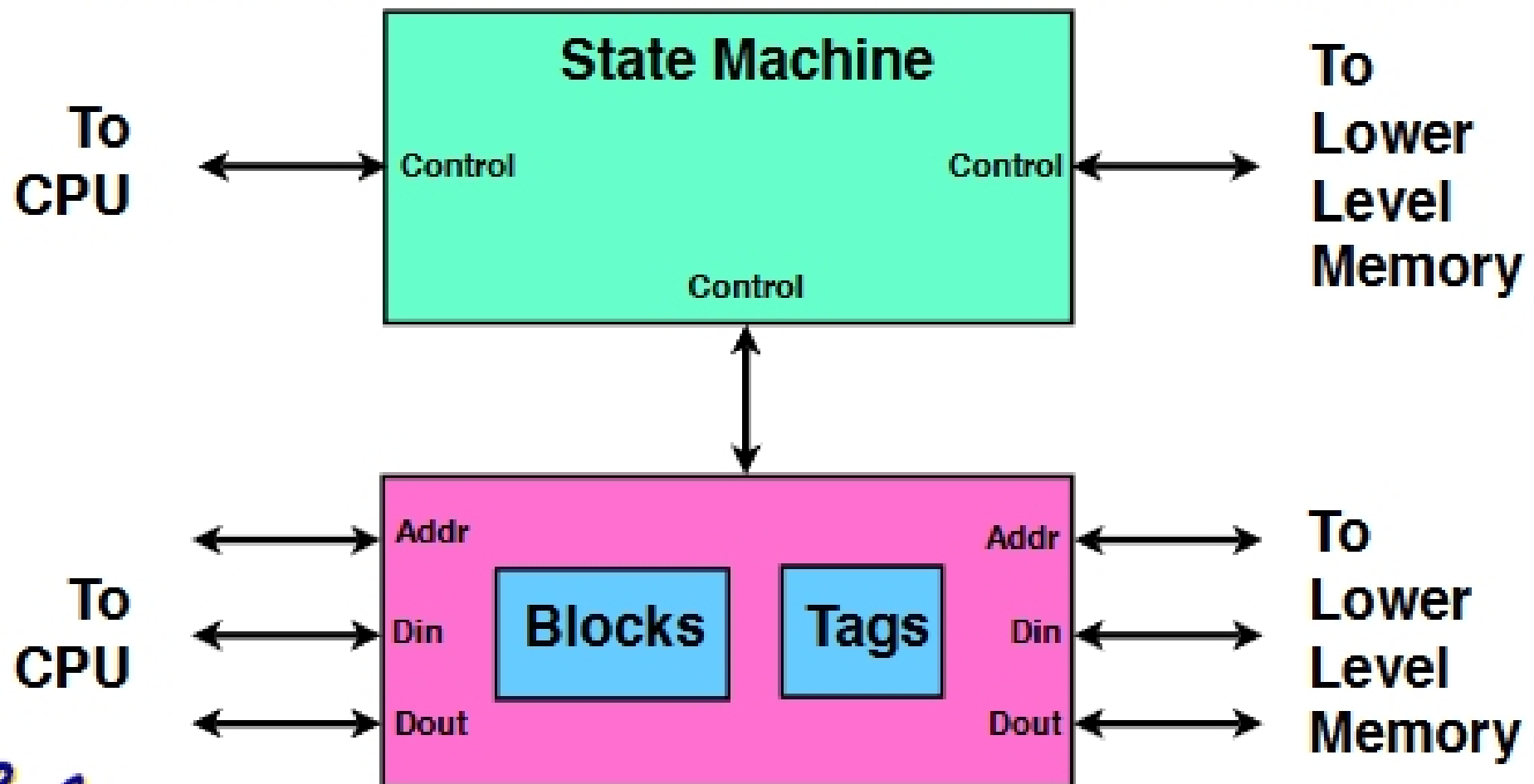
[www-inst.eecs.berkeley.edu/~cs152/](http://www-inst.eecs.berkeley.edu/~cs152/)



# Last Time: How to Design a Cache

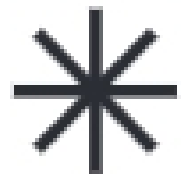
Most design errors come from incorrect specification of state machine behavior!

Common bugs: stalls, block replacement, write buffer



# Today's Lecture - Virtual Memory

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**DRAM technology**



**Virtual address spaces**



**Page table layout**



**TLB design options**

