EE129 Computer Communication Networks

Fall Semester 2006

Project #2: Build Serial Transceiver

Summary:

You are to design and implement the Serial Transmitter and Receiver in Verilog Hardware Description Language. The design will be synthesized by Altera Quartus II software and download to DE2 FPGA development board.

Description:

Design the transmitter and receiver module with following parameters:

- Baud Rate = 115200
- No Parity Check
- 8 Bits for data
- 1 Stop Bit

Receiver Module:

The receiver module should declare as shown below:

```
module serialReceiver(clk, rxd, rxd_data, dataReady);
   input        clk;  //Clock signal from DE2 board, its frequency is 50MHZ
   input        rxd;  //Receive Data Pin from serial port
   output [7:0] rxd_data;  //Parallel output for received data
   output       dataReady;  //Signal new data is ready with a low to high transition
   ...
endmodule
```

Since clock signal is not send along with data over serial port, receiver module has to use a clock from DE2 board to decode the received data.

- Implement it using state machine.
- Sample waveform for each bit 8 times (as shown in Figure 1).
- Derive the sampling clock pulse from main 50MHZ clock.

Figure 1. Serial Data

The timing diagram for receiver module is shown in figure 2. When a new byte is received and decoded, the rxd_data should be set to new byte first; then dataReady have a positive edge transition. The rxd_data should not change until next byte is received and decoded.

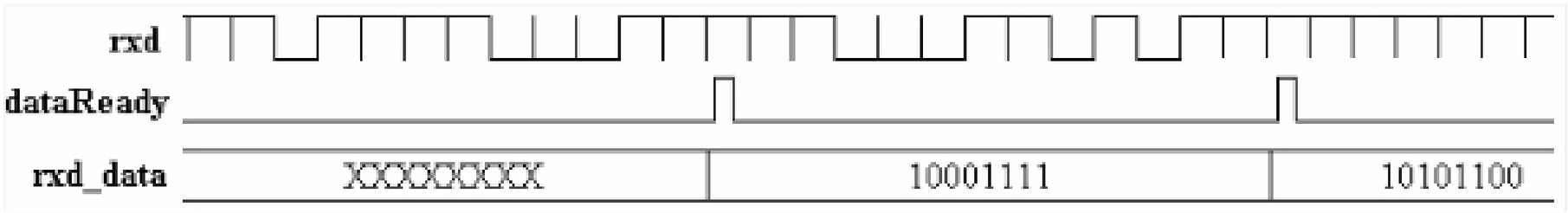

Figure 2. Receiver Module Timing Diagram

Transmitter Module

The transmitter module should declare as shown below:

```
module serialReceiver(clk, txd_data, txd_start, txd, txd_busy);
    input        clk;  // Clock signal from DE2 board, its frequency is 50MHZ
    input [7:0]  txd_data;   //Parallel data to be sent over serial port.
    input        txd_start;  //A low to high transition to signal start of data transmission.
    output       txd;  //Transmit Data Pin from serial port
    output       txd_busy;  //This pin stay high when transmitter is transmitting data.
    ...
endmodule
```

For transmitter module, txd_busy pin become high when ever transmitter is transmitting serial data. At idle state (when there is nothing to send), txd pin should be high (as shown in Figure 3).

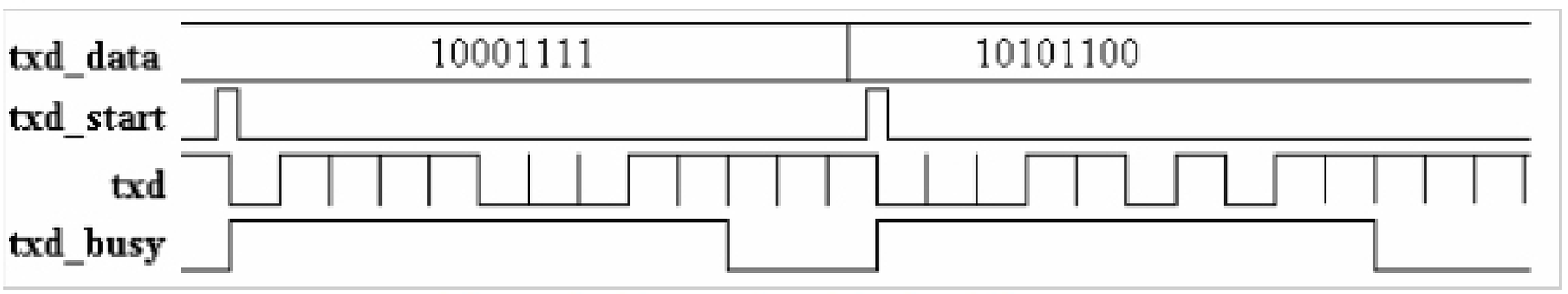

Figure 3. Transmitter Timing Diagram

Report:

Submit the follows:

- the source codes signed by TA
- timing simulation of for two modules

Other useful information:

The Altera Quartus II software is installed in computer lab 120 with license file located at *26000@eecsdc01*. Or you can install it to your own computer, the link for software and license download is posted on course website.

The serial transceiver module will also be interfaced with LCD, 7-segment LEDs and LEDS. Codes for those modules and tutorial for using Quartus II software is also posted on course website.

Implementation and report is due on Thursday, November 30, 2006.