

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.012
Microelectronic Devices and Circuits
Spring 2009

Design Project

This project may be worked on in groups of two. If you choose to work with a partner, turn in one report for both partners. The design process is long – start working early.

1 The Optical Converter

Information can be encoded and transmitted optically. Such a data transmission system requires a decoding receiver that converts the information contained in the intensity of transmitted photons into useful electrical signals understandable by digital processors. You will be designing a converter from photons to a pulse width modulated signal to be used as the first stage of a four-state optical receiver.

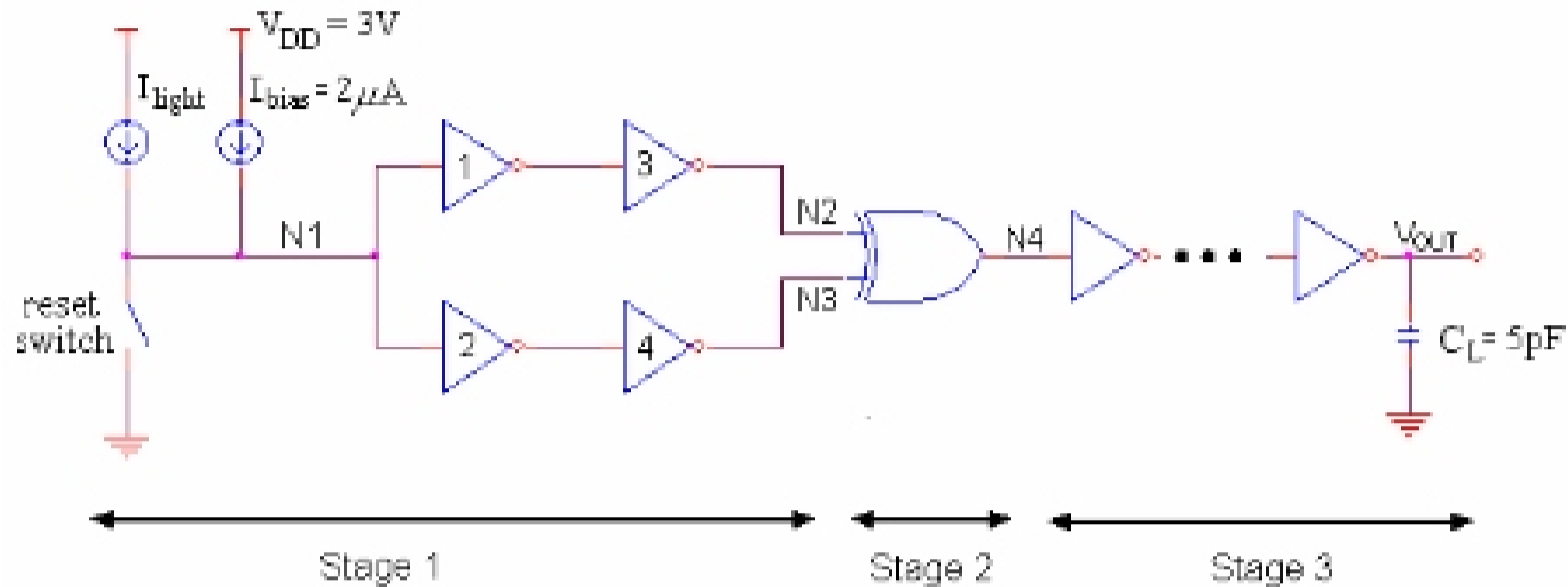
Our converter will generate pulses of four different widths in time, corresponding to the four light intensity levels the receiver detects. We will design for a 200MHz receiver system clock speed. The four pulses must be wide enough to allow for several clock cycles to complete in one pulse, and sufficiently distinct in width from each other for each of the four pulses to be differentiated by the next stage of the receiver, which counts the number of clock cycles within a pulse.

The converter should be designed in three stages:

1. **Stage 1** detects the incoming photon intensity and converts it into a current signal. A photodiode is a device that passes a current that is directly proportional to the detected light intensity. This current is used in the generation of two voltage steps, where the time delay between the two steps is a function of the photodiode current.
2. **Stage 2** converts the time delayed voltage steps to a single pulse, whose pulse width is the time delay between the two outputs from Stage 1.
3. **Stage 3** is an output buffer that is designed to drive a 5pF load capacitance.

As electronics trend ever smaller and more portable, die area has become an increasingly important design parameter for circuit designers. In this project, we will focus our design efforts on minimizing total gate area while preserving desired functionality.

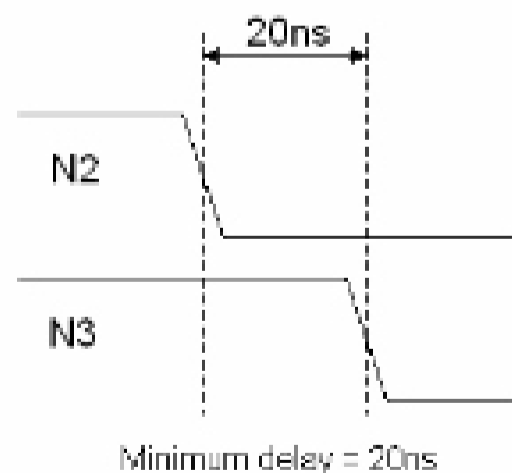
2 Implementation



2.1 STAGE 1

We will model the photodiode in our circuit as an ideal four level current source that sources $I_{light} = 0\mu A, 1\mu A, 2\mu A,$ and $3\mu A$, with $0\mu A$ corresponding to a completely dark input. A bias current source of $I_{bias} = 2\mu A$ is placed in parallel with the photodiode. The two current sources sum and drive the capacitance seen at node N1, which will be the sum of gate capacitances of inverters 1 and 2. An ideal voltage controlled switch connects N1 to ground. When the switch is closed, node N1 sees a direct path to ground. When the switch is open, the current sources charge the capacitances at N1, producing a voltage ramp at that node. The difference in V_M between inverters 1 and 2 produce the time delay between the steps at N2 and N3. Inverters 3 and 4 clean up the output signals from inverters 1 and 2.

Your task is to design the four inverters 1–4. To maintain compatibility with the 200MHz system clock, the time delay between voltage steps generated in this stage should be no less than 20ns. The minimum difference between time delays generated by different light intensities should also be 20ns. That is, if at some I_{light} the generated delay is 20ns, then at the next I_{light} level, the time delay should be no less than 40ns, and so on.



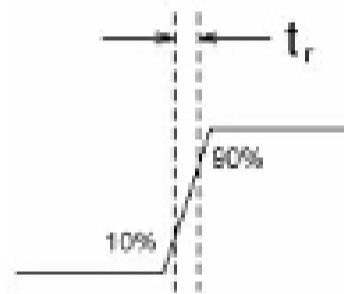
High gain inverters 1 and 2 should be sized to achieve the appropriate V_M and gate capacitance, chosen to achieve the delay specifications while trying to minimize the total gate area of Stage 1. Your project will be evaluated based on how low gate area you achieve, which should not exceed $400\mu\text{m}^2$.

2.2 STAGE 2

Stage 2 takes as inputs the time delayed steps from Stage 1, and outputs a single pulse whose width is the time delay between the two Stage 1 steps. A device that can accomplish this is an XOR gate. Show using a truth table why this is true. Your task is to design an XOR gate. The XOR gate should be composed of AND, OR gates, or their complements as well as inverters if needed.

2.3 STAGE 3

The output buffer is a chain of inverters designed to drive 5pF . Your task is to determine how many and what size inverters are necessary to drive 5pF and generate a positive going pulse at V_{OUT} . The inverters should be individually sized to drive the increasing load capacitance seen at the output of each subsequent inverter. Rise and fall times at V_{OUT} should each not exceed 3ns , measured from the 10% to 90% points.



The total gate area for stage 2 and 3 should not exceed $600\mu\text{m}^2$, and as with Stage 1, you should try to achieve as low gate area as you can design.

2.4 SUMMARY OF SPECIFICATIONS

Supply	$V_{DD} = 3\text{V}$		
Stage 1	Maximum gate area	400	μm^2
	Minimum pulse width	20	ns
	Minimum output step size	20	ns
Stage 2&3	Maximum total gate area	600	μm^2
Stage 3	Maximum t_r, t_f	3	ns
	Load capacitance	5	pF