CS152
Computer Architecture and Engineering
Lecture 4

Cost and Design

September 12, 2001

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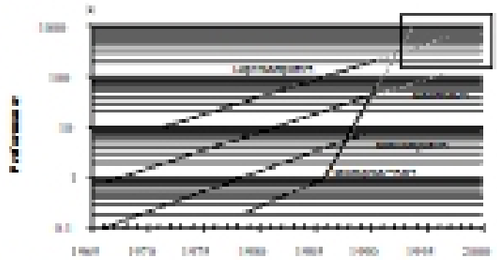
lecture slides: http://www-inst.eecs.berkeley.edu/~cs152/

Review: Performance and Technology Trends



° Technology Power: 1.2 x 1.2 x 1.2 = 1.7 x / year
- Feature Size: shrinks 10% / yr. => switching speed improves 1.2 / yr.
- Density: improves 1.2x / yr.
- Die Area: 1.2x / yr.

° RISC lesson is to keep the ISA as simple as possible:
- Shorter design cycle => fully exploit the advancing technology (~3yr)
- Advanced branch prediction and pipeline techniques
- Bigger and more sophisticated on-chip caches

Review: Characterize a Gate

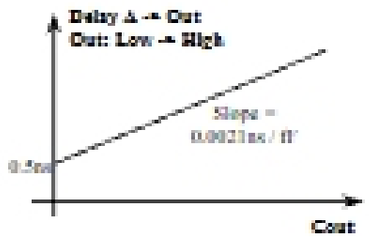
° Input capacitance for each input

° For each input-to-output path:
- For each output transition type (H->L, L->H, H->Z, L->Z ... etc.)
  - Internal delay (ns)
  - Load dependent delay (ns / fF)

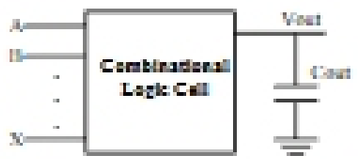
° Example: 2-input NAND Gate

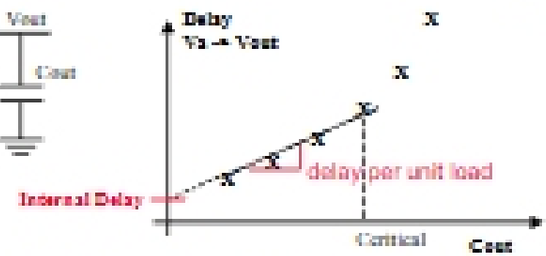
For A and B: Input Load (I.L.) = 61 fF

For either A -> Out or B -> Out:
Tlh = 0.5ns Thl = 0.0021ns / fF
Thl = 0.3ns Thlf = 0.0020ns / fF



Review: General C/L Cell Delay Model

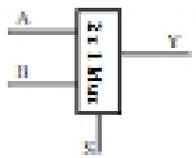




° Combinational Cell (symbol) is fully specified by:
- functional (input -> output) behavior
  - truth-table, logic equation, VHDL
- load factor of each input
- critical propagation delay from each input to each output for each transition
  - $T_{IL}(A, o)$ = Fixed Internal Delay + Load-dependent-delay x *load*

° Linear model composes

Review: More complicated gates



° Three Components:
- Input Load
- Load Dependent Delay
- Internal Delays
  - One for each input path→output transition

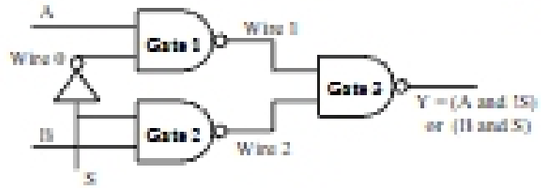
° Input Load: A = 61 fF, B = 61 fF, S = 111 fF

° Load Dependent Delay:
- TAYlnf = 0.0021 ns / fF TAYhlf = 0.0020 ns / fF
- TBYlnf = 0.0021 ns / fF TBYhlf = 0.0020 ns / fF
- TSYlnf = 0.0021 ns / fF TSYlnf = 0.0020 ns / f F

° Internal Delay:
- TAYlh = 0.844ns TBYlh = 0.844ns
- Fun Exercises: TAYhl, TBYhl, TSYlh, TSYlh

° How do we compute these numbers?

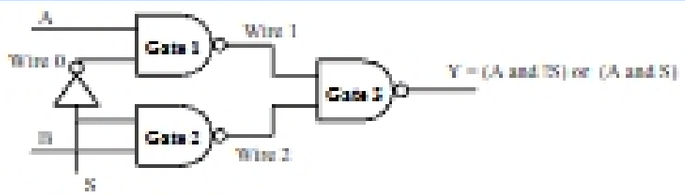
2 to 1 MUX: Input Load and Load Dependent Delay



° Input Load (I.L.)
- A, B: I.L. (NAND) = 61 fF
- S: I.L. (INV) + I.L. (NAND) = 50 fF + 61 fF = 111 fF

° Load Dependent Delay (L.D.D.): Same as Gate 3
- TAYlnf = 0.0021 ns / fF TAYhlf = 0.0020 ns / fF
- TBYlnf = 0.0021 ns / fF TBYhlf = 0.0020 ns / fF
- TSYlnf = 0.0021 ns / fF TSYlnf = 0.0020 ns / fF

2 to 1 MUX: Internal Delay Calculation



° Internal Delay (I.D.):
- A to Y: I.D. G1 + (Wire 1 C + G3 Input C) * L.D.D G1 + I.D. G3
- B to Y: I.D. G2 + (Wire 2 C + G3 Input C) * L.D.D. G2 + I.D. G3
- S to Y (Worst Case): I.D. Inv + (Wire 0 C + G1 Input C) * L.D.D. Inv + Internal Delay A to Y

° We can approximate the effect of "Wire 1 C" by:
- Assume Wire 1 has the same C as all the gate C attached to it.

° Specific Example:
- TAYlh = TPhl G1 + (2.0 * 61 fF) * TPhlf G1 + TPlh G3
  = 0.1ns + 122 fF * 0.0020 ns/fF + 0.6ns = 0.844 ns

CS152 Logic Elements

° NAND2, NAND3, NAND 4

° NOR2, NOR3, NOR4

° INV1x (normal inverter)

° INV4x (inverter with large output drive)

° XOR2

° XNOR2

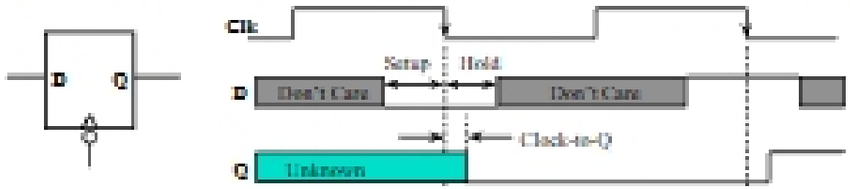
° PWR: Source of 1's

° GND: Source of 0's

° fast MUXes

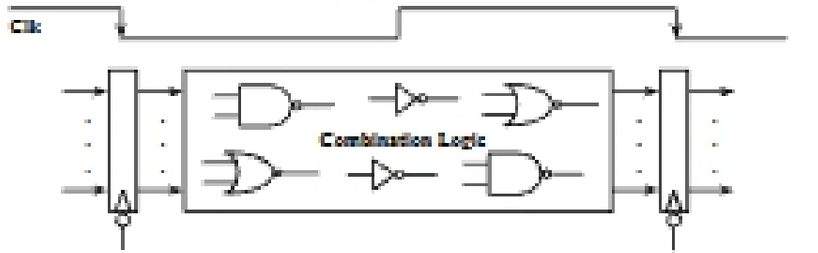
° D flip flop with negative edge triggered

Storage Element's Timing Model



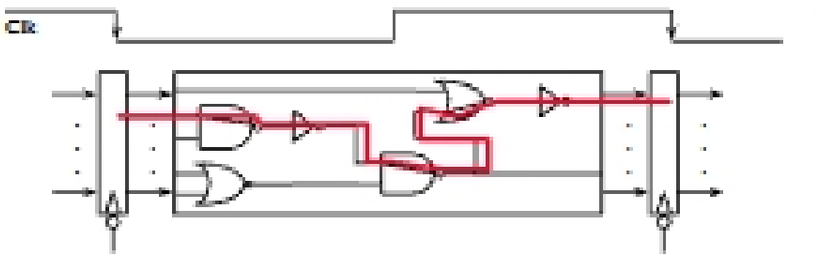
- Setup Time: Input must be stable BEFORE the trigger clock edge
- Hold Time: Input must REMAIN stable after the trigger clock edge
- Clock-to-Q time:
  - Output cannot change instantaneously at the trigger clock edge
  - Similar to delay in logic gates, two components:
    - Internal Clock-to-Q
    - Load dependent Clock-to-Q
- Typical for class: 1ns Setup, 0.5ns Hold

Clocking Methodology



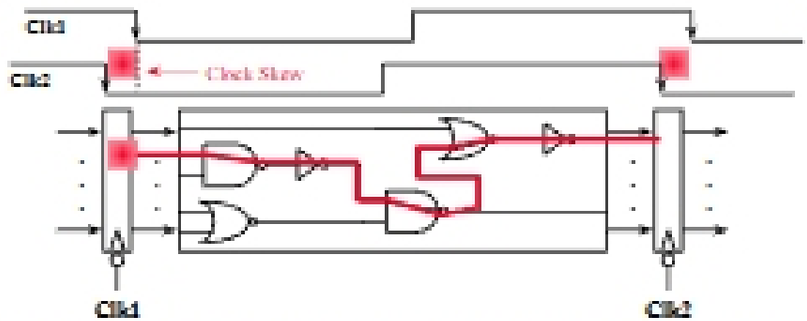
- All storage elements are clocked by the same clock edge
- The combination logic block's:
  - Inputs are updated at each clock tick
  - All outputs MUST be stable before the next clock tick

Critical Path & Cycle Time



- Critical path: the slowest path between any two storage devices
- Cycle time is a function of the critical path
- must be greater than:
  - Clock-to-Q + Longest Path through Combination Logic + Setup

Clock Skew's Effect on Cycle Time



- The worst case scenario for cycle time consideration:
  - The input register sees CLK1
  - The output register sees CLK2
- Cycle Time - Clock Skew ≥ CLK-to-Q + Longest Delay + Setup
  ⇒ Cycle Time ≥ CLK-to-Q + Longest Delay + Setup + Clock Skew