

Statistical Counters

A brief look at our Intel gigabit ethernet network controller's 'event-counting' registers

Statistics registers

- The 82573L has several dozen statistical counters which automatically operate to keep track of significant events affecting the ethernet controller's performance
- Most are 32-bit 'read-only' registers, and they are automatically cleared when read
- Your module's initialization routine could read them all (to start counting from zero)

Initializing the nic's counters

- The statistical counters all have address-offsets in the range 0x04000 – 0x041FF
- You can use a very simple program-loop to 'clear' each of these read-only registers

```
// Here 'io' is the virtual base-address of the nic's i/o-memory region
{
    int    r;

    // clear all of the Pro/1000 controller's statistical counters
    for (r = 0x4000; r < 0x41FF; r += 4) ioread32( io + r );
}
```