VIRGINIA COMMONWEALTH UNIVERSITY

SCHOOL OF ENGINEERING

EGRE 427 **Spring 2001**

Advanced Digital Design

Credits: 4 (3 hours lecture, 3 hours laboratory)

Prerequisites: EGRE 426 Computer Organization and Design

Instructor: Dr. Robert Klenke, Course Director
Phone: 827-7007 Email: rhklenke@vcu.edu
Office Hours: T,R 1:00 – 2:00

Course Web Page: http://www.people.vcu.edu/~rhklenke/egre427/index.html

Course Text: Michael John Sebastian Smith : *Application-Specific Integrated Circuits;* Addison-Wesley, 1997.

Course Description:

This is an elective course in the computer engineering sequence that provides students with practical foundations for the design, implementation, and testing of digital systems. It expands on the digital and computer system theory presented in prerequisite courses.

Topics covered include, microcontrollers and embedded processors, application specific IC (ASIC) architectures and implementing digital systems with ASICs, logic synthesis, design methodologies, hardware/software codesign, production testing and design for testability, and construction, testing, and debugging of digital system prototypes. In the laboratory, the students will design, construct, test and debug a multidisciplinary, computer-based, hardware/software system for their senior design project. In order to master the material being covered during the semester, drill problems will be assigned in addition to the presented lecture material. The drill problems should be completed concurrently with the lecture material. The problems will be graded, and solutions will be made available.

Course Objectives

Upon successful completion of this course, the student will be able to:

1. Understand the typical features of an embedded microcontroller and how they are applied in controling real-time systems.
2. Write synthesizable behavioral VHDL descriptions of combinational and sequential logic and map them to a gate-level implementation using automatic synthesis tools
3. Understand the types of Application Specific Integrated Circuit (ASIC) devices available, including PLDs and FPGAs, what their internal architecture is, and how that influences their use in implementing digital systems
4. Understand the goals of production testing of digital devices and some of the tools and techniques used to perform it.
5. Understand what hardware/software partitioning and codesign is and some of the tools and techniques used to perform it.
6. Design, construct, test and debug a computer-based hardware/software system.

The course laboratory exercises involve becoming familiar with the use of Mentor Graphics and Actel commercial EDA tools used for designing and implementing a digital system in an FPGA, the use of the Microchip tools for developing software for a PIC microcontroller, and other tools such as the Tektronix TLA 714 logic analyzer used to actually build and test a digital system. Much of the laboratory time will be devoted to working on the student's capstone design project in the computer engineering area.

A course syllabus detailing the course plan, topical contents, and assignments is attached.

Laboratory Exercises

As stated above, the lab exercises are designed to help you learn the tools that will be used to design and implement you senior design project. **Attendance at the laboratory periods is mandatory and a class/lab participation grade will be give that will be partially based on attendance. Successful completion of all lab exercises is required to pass this course.**

Each formal lab exercise will be documented by the student with a lab write-up. The lab write-up should include the following items: 1) a brief description of lab objective and process, 2) a printout of all schematics and plots of the lab results, 3) a brief analysis of the results of the lab, 4) a description of any problems encountered, recommendations for changes, or improvements to the lab exercise. All lab exercises must be typeset and submitted in hardcopy.

Course Grading Policy

Final course grades will be determined as follows:

Midterm	15%
Homework/Laboratory	20%
Class Participation	5%
Design Project	45%
Final exam	15%

There is a 10%/day "penalty" on the grade for late assignments. Class participation grade will be determined from lecture and lab attendance and the student's participation in the in-class discussions.

Engineering Portfolios

As part of the ABET accreditation process, each student is required to maintain a portfolio of major assignments in each of their classes. For this course, the portfolio must contain, at a minimum, one of the lab write-ups and the final design project write-up.

University Policy on Cheating and Plagiarism

It is imperative that all graded assignments that you turn in during the course reflect your own understanding of the material. Copying answers from another person impedes the learning process and compromises your integrity. Students are encouraged to discuss homework problems and laboratory assignments with others, but submitted solutions must involve only an individual's effort. Any student who copies from another student's homework, quiz, exam, report, etc., or any student who knowingly allows another student to copy his or her work, or any student who submits someone else's work as his or her own, will be deemed guilty of cheating. Cheating is an extremely serious offense. Each student is expected to have read and understood the VCU Honor System Policy, as set forth in the 1998-99 VCU Resource Guide published by the Division of Student Affairs.