

EECS150 - Digital Design

Lecture 9- CPU Microarchitecture

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John Wawrzynek

Watson: Jeopardy-playing Computer



Watson is made up of a cluster of ninety IBM Power 750 servers (plus additional I/O, network and cluster controller nodes in 10 racks) for a total of 2880 POWER7 processor cores and 16 Terabytes of RAM. Each Power 750 server uses a 3.5 GHz POWER7 eight core processor, with four threads per core, and it still takes ~15 seconds a question.

Each core can do 8 double-precision FLOPS/cycle. So total is $2880 \cdot 3.5 \cdot 8 > 80$ TFLOPS

Processor Microarchitecture Introduction

Microarchitecture: how to implement an architecture in hardware

Good examples of how to put principles of digital design to practice.

Introduction to final project.

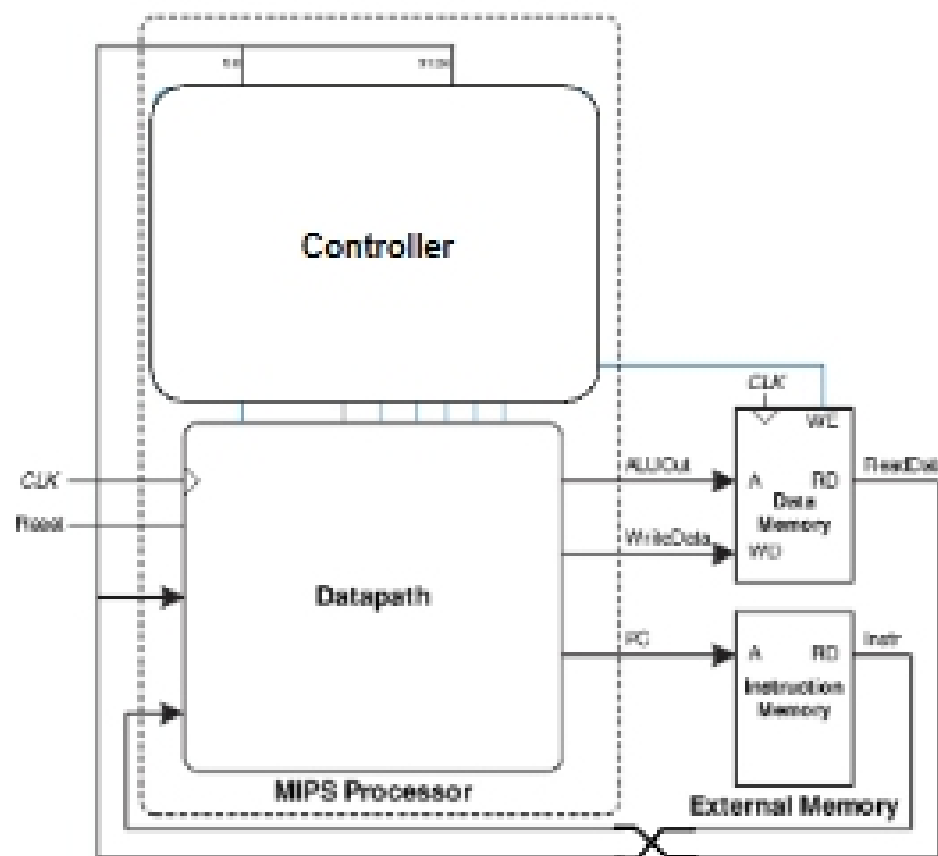
Application Software	programs
Operating Systems	device drivers
Architecture	instructions registers
Micro-architecture	datapaths controllers
Logic	adders memories
Digital Circuits	AND gates NOT gates
Analog Circuits	amplifiers filters
Devices	transistors diodes
Physics	electrons

MIPS Processor Architecture

- For now we consider a subset of MIPS instructions:
 - R-type instructions: `and`, `or`, `add`, `sub`, `slt`
 - Memory instructions: `lw`, `sw`
 - Branch instructions: `beq`
- Later we'll add `addi` and `j`

MIPS Micrarchitecture Organization

Datapath + Controller + External Memory



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How to Design a Processor: step-by-step

1. Analyze instruction set architecture (ISA) \Rightarrow datapath [requirements](#)
 - meaning of each instruction is given by the *data transfers (register transfers)*
 - datapath must include storage element for ISA registers
 - datapath must support each data transfer
2. Select set of datapath components and establish clocking methodology
3. Assemble datapath meeting requirements
4. Analyze implementation of each instruction to determine setting of control points that effects the data transfer.
5. Assemble the control logic.

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