CS152 – Computer Architecture and Engineering

Lecture 6 – Single Cycle + Design Notebook

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Review

- Timing key concept: critical path

- Xilinx: Physical, yet configurable

Outline

- Single clock cycle per instruction

  => Data path resource used at most once per instruction

  => Need to replicate some data path resources if need more than once: memory, ALU/adders, …

- Timing, Testing of Single Cycle
- Single Cycle Datapath
  - 5 generic steps (on next slide)
  - See how far we get this lecture; finish next time
- Design Notebook