3.4 Addressing modes

Specify the operand to be used. To generate an address, a segment register is used also.

Immediate addressing: the operand is a number included in the instruction body.

Register addressing: the operand is a register.

MOV CX,1024

ADD AL , BL

Direct addressing: the operand address is a number in [] or the value of a symbol (no [].)

MOV AX,[3000]

MOV BL,COUNTER

Register indirect addressing: the register enclosed in [ ] specifies the operand address.

Indexed addressing: the operand address is the sum of the value of the index register and a number, both enclosed in [ ].

MOV BX,[SI]

MOV BX,[SI + 10]

MOV CL,[BP - 4]

The displacement is a signed 2's complement byte or word

Based addressing: is similar to indexed, but using BP (base pointer) register.

Based-indexed addressing: the operand address is the sum of the values of BP and one of the index registers (SI or DI).

MOV DS:[BP + DI],AX

Segment overriding

Based-indexed with displacement addressing: ads to the former an offset value.

MOV DL,[BP][DI + 2] or MOV DL,[BP + DI + 2]

Port addressing: used by input/output instructions. The address of the source port for IN or destination port for OUT is a number or a register content.

OUT 80H , AL

IN AL, DX

3.5 The Processor Flags (Condition Codes)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	NT	IOPL		OF	DF	IF	TF	SF	ZF	-	AF	-	PF	-	CF

CF	Carry Flag	Contains Carry out of MSB of result	Condition Code half
PF	Parity Flag	Indicates if result has even parity	
AF	Auxiliary carry Flag	Contains Carry out of bit 3 in AL	
ZF	Zero Flag	Indicates if result equals zero	
SF	Sign Flag	Indicates if result is negative	
TF	Trace Flag	Provides a single step capability for debugging	Additional Flags
IF	Interrupt enable Flag	Enables/disables interrupts	
DF	Direction Flag	Controls pointer updating during string operations	
OF	Overflow Flag	Indicates that an overflow occurred in result	
IOPL	I/O Priority Level	Priority level of current task (two bits)	
NT	Nested Task	Indicates if current task is nested	

3.5 The Processor Flags (Condition Codes)

Sign (Bit 7)

Represent the sign (2's complement) of the last arithmetical or logical operation.

The MSB (Most Significant Bit) of the last arithmetical or logical operation result.

Bit 7 for byte operation
Bit 15 for word operation
Bit 31 for double-word operation

The processor doesn't knows if the result is to be interpreted as "signed" or "unsigned". S flag is always generated. It is the programmer responsibility to test or not the S flag.

CMP (Compare) instruction is a subtraction without a saved result. Sign bit is affected.

Not affected by other types of instructions (i.e. MOV, JMP, etc)

Examples: