Reading Assignment: Section 2.10 in *Logic and Computer Design Fundamentals, 4th Edition* by Mano

Three-State Devices (Tri-State Devices)

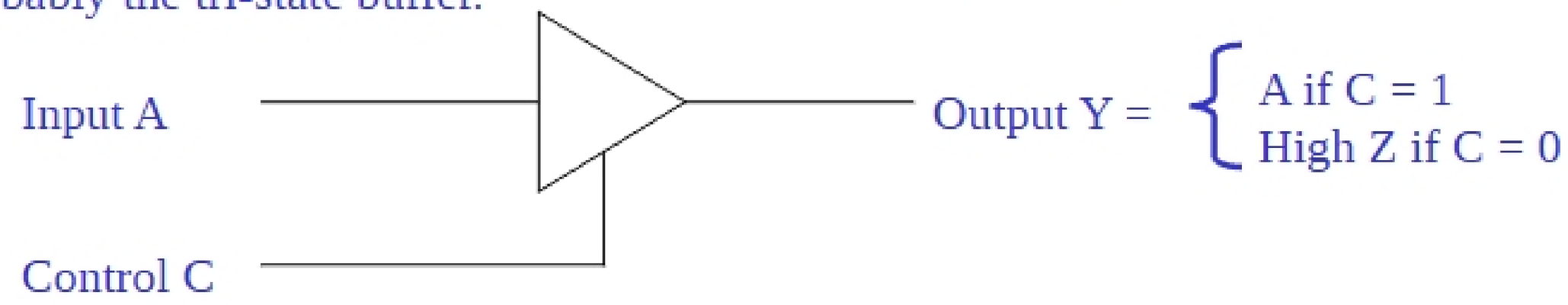
Devices used so far have two output states: logic 0 or logic 1

Tri-state devices have three output states:

1) Logic 0
2) Logic 1
3) High impedance (Z) state

When a tri-state device is in the high Z state, the output appears to be disconnected. This allows several outputs to be connected together, such as in the case where several outputs are connected to a common bus.

Although tri-state outputs are available with various types of gates, the most common is probably the tri-state buffer.



Tri-state buffer

The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

SN54125, SN54126, SN54LS125A, SN54LS126A, SN74125, SN74126, SN74LS125A, SN74LS126A
QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

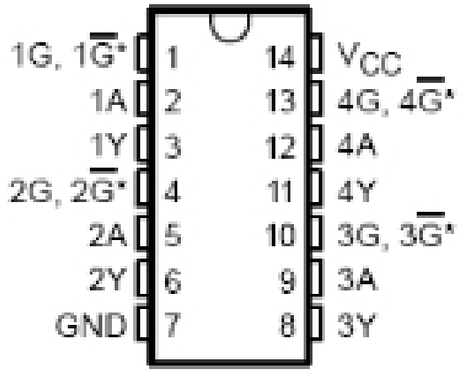
SDLS044A – DECEMBER 1983 – REVISED MARCH 2002

- Quad Bus Buffers
- 3-State Outputs
- Separate Control for Each Channel

description

These bus buffers feature three-state outputs that, when enabled, have the low impedance characteristics of a TTL output with additional drive capability at high logic levels to permit driving heavily loaded bus lines without external pullup resistors. When disabled, both output transistors are turned off, presenting a high-impedance state to the bus so the output will act neither as a significant load nor as a driver. The '125 and 'LS125A devices' outputs are disabled when $\overline{G}$ is high. The '126 and 'LS126A devices' outputs are disabled when G is low.

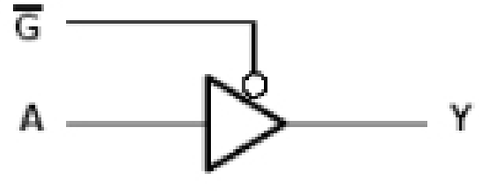
SN54125, SN54126, SN54LS125A, SN54LS126A . . . J OR W PACKAGE
SN74125, SN74126 . . . N PACKAGE
SN74LS125A, SN74LS126A . . . D, N, OR NS PACKAGE
(TOP VIEW)



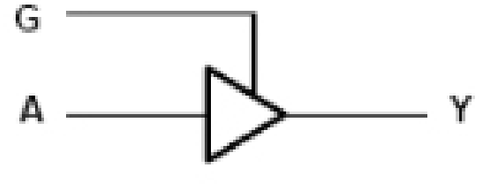
*$\overline{G}$ on '125 and 'LS125A devices;
G on 126 and 'LS126A devices

SN54LS125A, SN54LS126A . . . FK PACKAGE
(TOP VIEW)

'125, 'LS125A



'126, 'LS126A



Octal 3-state buffer:

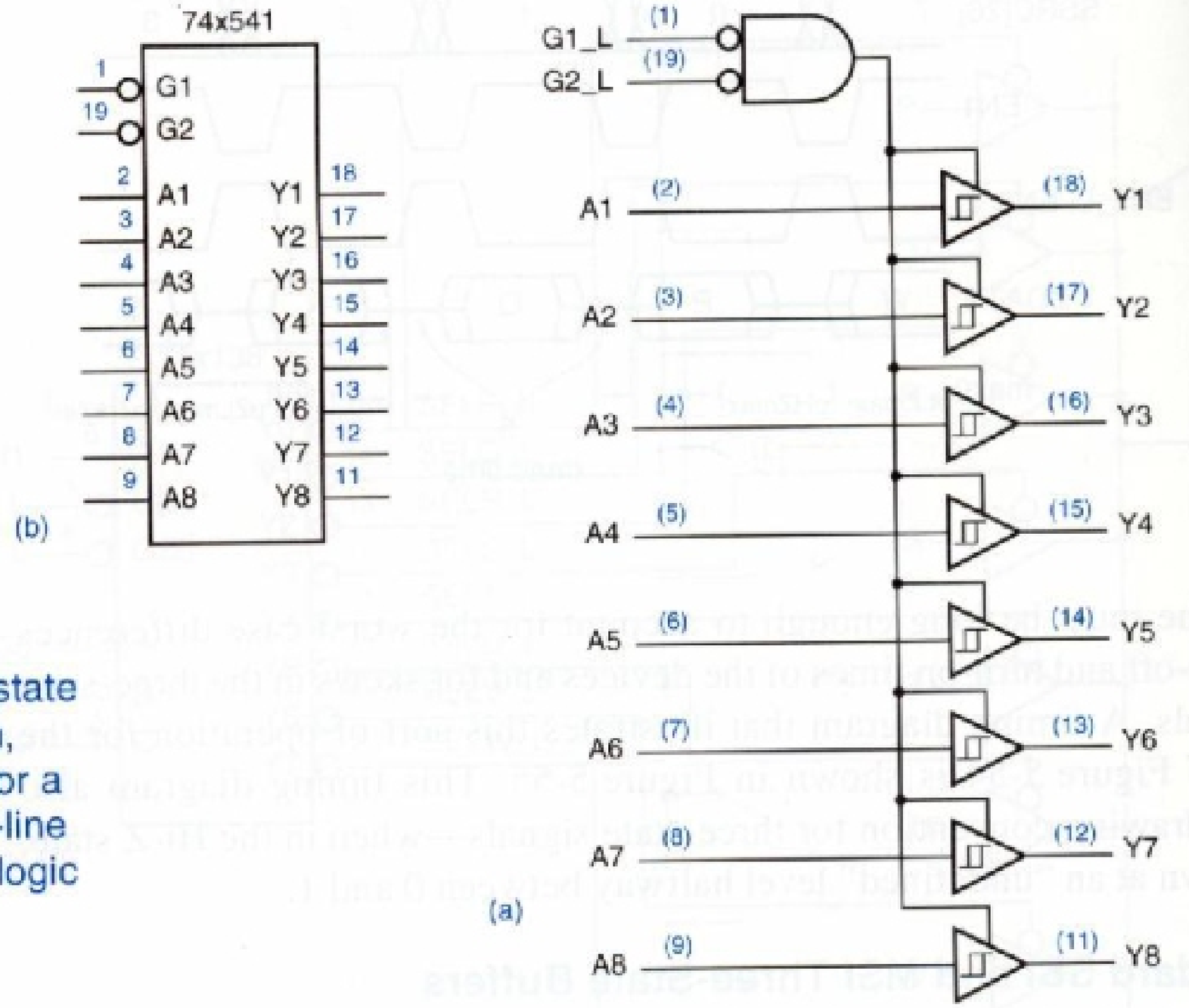


Figure 5-57
The 74x541 octal three-state buffer: (a) logic diagram, including pin numbers for a standard 20-pin dual in-line package; (b) traditional logic symbol.