EGRE 426
Digital Systems
Final
Closed Book/ Closed Notes
12/8/08
Counts as 1/3

NAME: SOLUTIONS

1. Hennessy and Patterson use a laundry analogy to help explain pipelining. Match the appropriate Flynn computer category model with the closest laundry analogy.

a. SISD

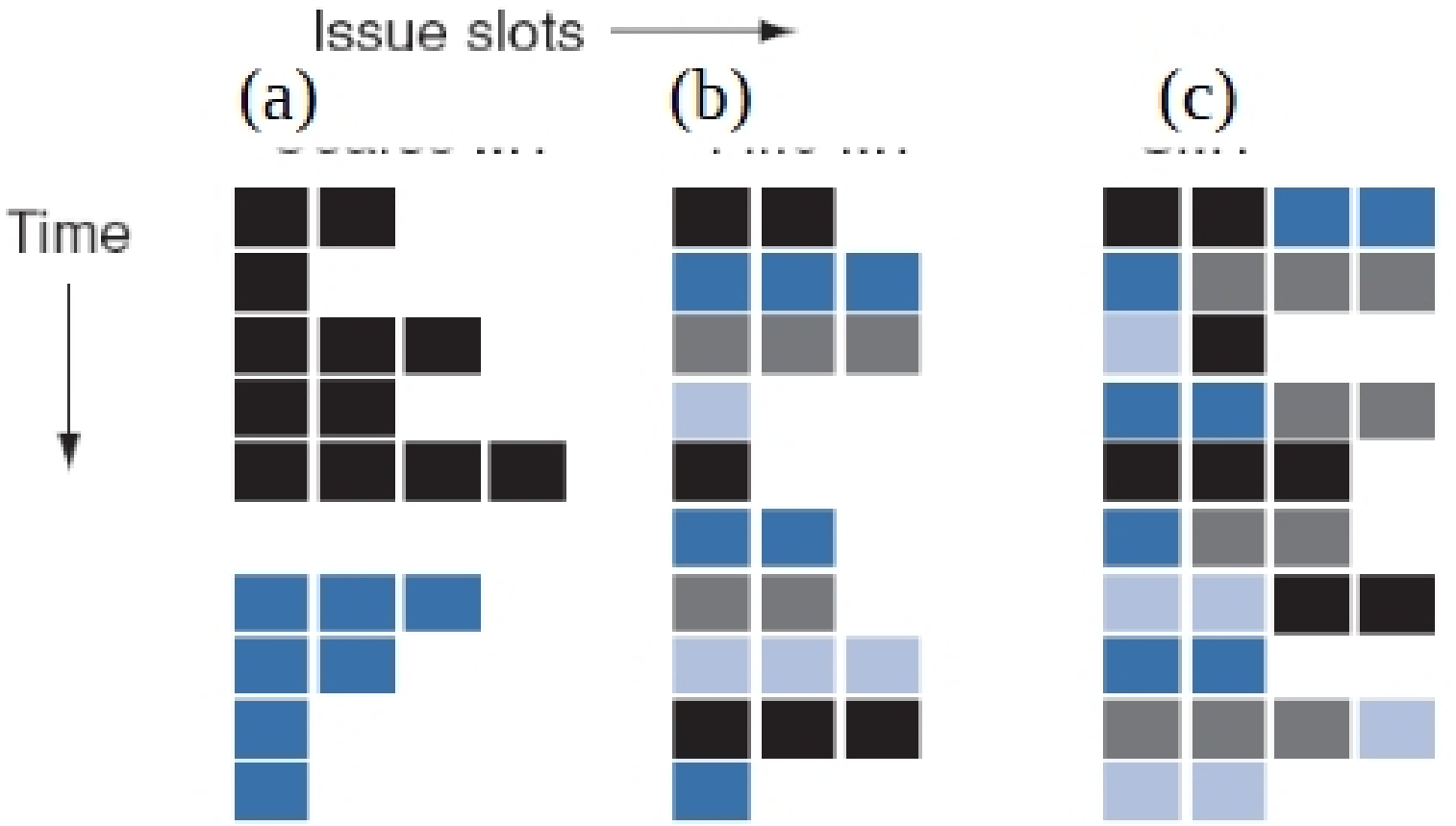
b. MIMD

c. SIMD

1. UVA - Boy Engineer puts bag of dirty clothes in a washer. When done, he puts the clothes in a dryer. After removing clothes from the dryer, he neatly folds them, caries them to his room. Irons them, and puts them in the proper draw.
2. Virginia Tech - Boy Engineer carries a semesters worth of dirty clothes to the laundry, puts them in many washing machines and when done puts the clean clothes in many dryers. After removing the clothes from the dryers, he is ready for next semester.
3. VCU - Boy Engineer takes three bags of dirty clothes, gives one bag to each of his girl friends, and lets them do his laundry.

2. The figure shown below was used to explain different typed of different types of multithreading. Enter a, b, or c in the table to associate each figure with the appropriate type of multithreading.

C	Simultaneous Multithreading
b	Fine-grain Multithreading
a	Course-grain Multithreading



Circle T for true, F for false.

3. T (F) Write-through should always be used to manage writes in virtual memory systems.
4. (T) F Write-through cache memories do not need a dirty bit.
5. T (F) Write-back cache memories do not need a dirty bit.
6. T (F) Write-through cache memories do not need a valid bit.
7. T (F) Write-back cache memories do not need a valid bit.
8. T F The MIPS processor is an example of a RISC processor.
9. T F Temporal locality describes a characteristic of program data.
10. T F Spatial locality describes a characteristic of program code.
11. T F At any one time a scalar pipeline may contain several instructions.
12. T F At any one time a superscalar pipeline may contain several instructions.
13. T F At any one time several instructions may exit a scalar pipeline.
14. T F At any one time several instructions may exit a superscalar pipeline.
15. T F Only instructions with an illegal op codes or instructions that attempt to access an illegal memory location are aborted.
16. T F Aborting an instruction will cause bubbles in a pipeline.
17. T F When an instruction stalls bubbles are created in a pipeline..
18. T F Dynamic pipelines enable stalled instructions to be bypassed.
19. T F Dynamic pipelines reduce bubbles.

20. Circle T for true or F for false: A direct mapped **instruction cache** is used in a single processor system.

(a). T (F) We would expect this instruction cache to contain a dirty bit.
(b). (T) F We would expect this instruction cache to contain a valid bit.
(c). T (F) We would expect this instruction cache to contain a least recently used bit.
(d). T (F) We would expect this instruction cache to use a write back replacement scheme.
(e). T F We would **not** expect this instruction cache to use write through.
(f). T F We would **not** expect this instruction cache to use write back.