Design of Optimized Engine for Direct Sequence Spread Spectrum Transceiver

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1. Introduction

The interference in the wireless communication channel leads to spreading of the data to be transmitted over the entire frequency range thereby making it resistant to noise. One of the popular techniques for spreading of the data is Direct Sequence Spread spectrum (DSSS). It is used in popular applications such as IEEE 802.11b and CDMA. The data that is to be transmitted wirelessly is multiplied with a high frequency pseudo-random noise (PN) sequence at the transmitter. This causes the spreading of the power spectral density. The basic building blocks of the transceiver unit in DSSS consist of a pseudo random sequence generator, Digital Matched filter, Delay locked loop which consists of a detector, loop filter and numerically controlled oscillator.

At the receiver side the data is again multiplied with the same PN sequence that is locally generated to recover back the original data symbols. The most sensitive part of a Direct Sequence Spread Spectrum system is the synchronization of the transmitter's pseudo random sequence to that of the receiver where an offset of even one chip cycle can result in noise rather than a de-spread symbol sequence. Our project mainly focuses at the design of a fast Direct Sequence Spread Spectrum engine such that there is a faster correlation between the pseudo random sequence at the transmitter and the receiver.

2. Theoretical Background for Direct Sequence Spread Spectrum

The basic building block of the DSSS transmitter is shown below. The symbol to be transmitted is multiplied with the PN sequence to generate the spread symbol. The symbols are converted to analog form and are transmitted after the modulation.