Monday, April 18, 2005
EE 105 Discussion Section 101

Announcements

High Voltage Gain Amplifier Design

Suppose that it is desired to design an amplifier with large voltage gain using a single stage. Based upon our knowledge of single-stage amplifiers, one potential candidate is the common-source amplifier. Let's examine the maximum attainable voltage gain from such a stage.

Basic common-source amplifier

Figure 1 shows the circuit diagram of a PMOS common-source stage. The voltage gain of such a stage can be shown to equal the following,

$$\frac{v_{out}}{v_{in}} = -g_{m1} \cdot r_{o1} \qquad (1)$$

In order to obtain a feel for how high the expression in (1) can be in value, let's use appropriate equations for g_{m1} and r_{o1}. More specifically, substituting $g_{m1} = \frac{2 \cdot I_{SD1}}{V_{DSAT1}}$ and $r_{o1} = \frac{1}{\lambda_1 \cdot I_{SD1}}$ in (1) yields the following

$$\frac{v_{out}}{v_{in}} = -\frac{2 \cdot I_{SD1}}{V_{DSAT1}} \cdot \frac{1}{\lambda_1 \cdot I_{SD1}} = -\frac{2}{V_{DSAT1} \cdot \lambda_1} \qquad (2)$$

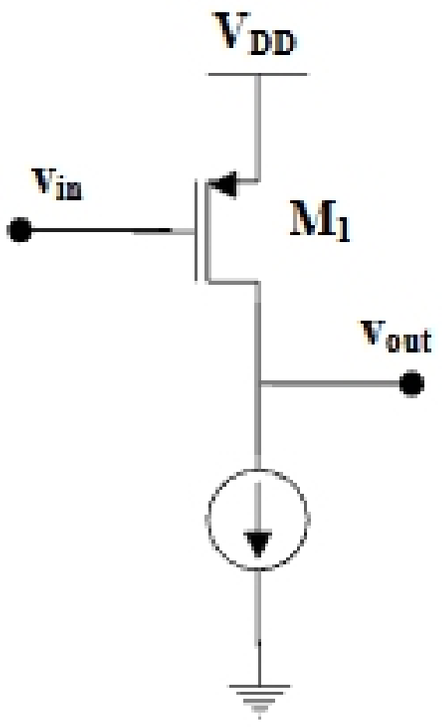

Figure 1. PMOS CS with ideal current source

Substituting typical values for V_{DSAT1} (200mV) and λ_1 ($0.05V^{-1}$) into (2), yields a voltage gain of 200 in magnitude. In order to increase the voltage gain of a common-source stage, one has two options from (2):

1. Reduce V_{DSAT1}, and/or
2. Reduce λ_1

Unfortunately, one can not reduce V_{DSAT1} endlessly because the MOSFET transistor enters the subthreshold region of operation (see EE 130) for V_{DSAT} values below approximately 150mV. This is why 100-150mV is often set as the lower bound for V_{DSAT} in when it comes to amplifier design in EE105/140/240. Hence, to increase the voltage

gain of a common-source stage beyond 200 in magnitude, one can only reduce λ in practice.

In order to reduce λ of a transistor, one needs to increase the length. In order to not upset the corresponding V_{DSAT} of the resulting transistor, one needs to increase the width by the same proportion. As an example, to increase the voltage gain of a common-source stage from 200 to 40E3, one would need to increase the length (and correspondingly width) by a factor of 200. Increasing the size of a transistor has two disadvantages: (i) eats up silicon area, (ii) degrades the frequency response because the intrinsic capacitances associated with the MOSFET are larger. The latter is of much more concern. Hence, a different topology needs to be employed if voltage gain larger than 200 in magnitude is desired.

Note: In practice, one does not have access to ideal current sources. As a result, the ideal current source depicted in Figure 1 would be implemented using a current mirror in practice. Subsequent to this, the voltage gain expression in (1) would need to be modified. The result is the following

$$\frac{v_{out}}{v_{in}} = -g_{m1} \cdot (r_{o1} \;//\; r_{o3}) \qquad (3)$$

where,

r_{o3} **is the resistance "looking" down into the current mirror-based current source.**

Cascode amplifier

In order to arrive at a topology that yields large voltage gain, one needs to step back and recall the big picture of how voltage gain is set. As mentioned on previous occasions, the voltage gain of an unloaded amplifier is given by the following expression

$$A_v = unloaded \;\; voltage \;\; gain = -G_m \cdot R_{out} \quad (4)$$

From (4), one has two options to increase the voltage gain of an amplifier:

1. Increase G_m, and/or
2. Increase R_{out}

Here, we will focus on the latter option, i.e. increasing the output resistance. The resulting amplifier is referred to as a **cascode amplifier**, a schematic of which is shown in Figure 2. Let's next examine the voltage gain of such a structure by evaluating, in turn, its G_m and R_{out}.

G_m of a cascode amplifier

Figure 3 shows the circuit from which G_m for the cascode amplifier shall be computed. Note that a test voltage (i.e. v_t) has been applied to the gate and the output has been shorted to ground, in accordance with the rules for calculating G_m. G_m can be calculated

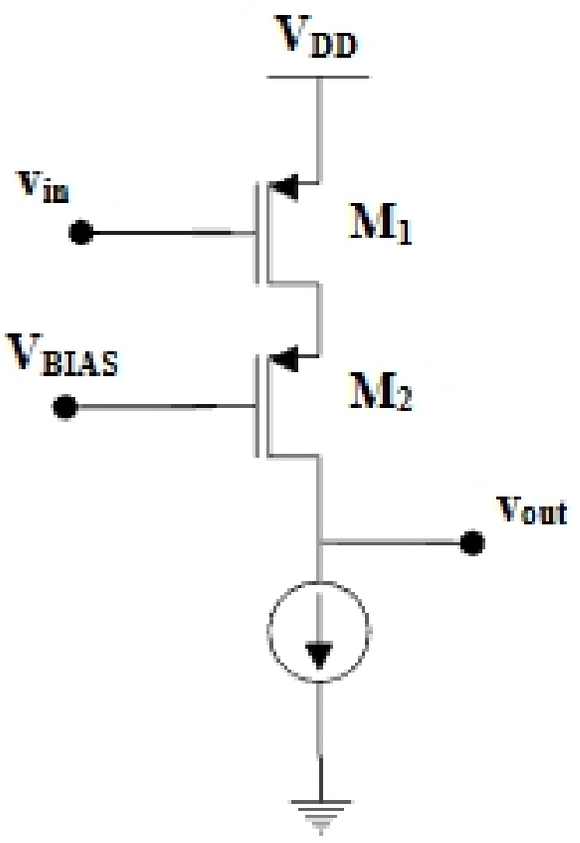

Figure 2. PMOS cascode with ideal current source

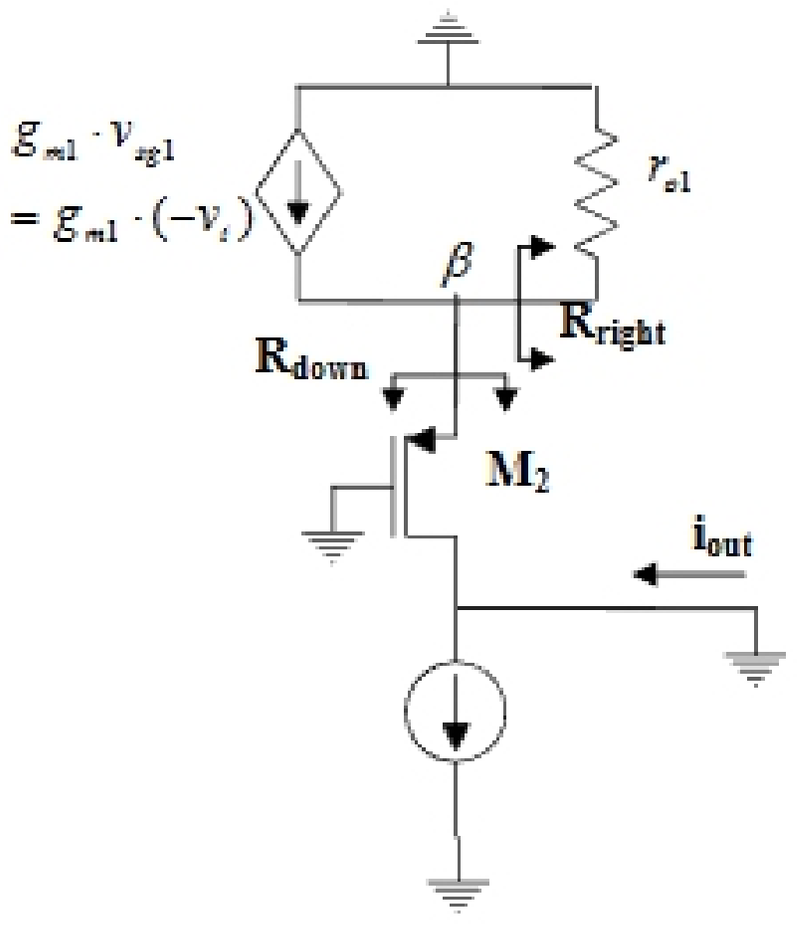

Figure 3. Calculating G_m

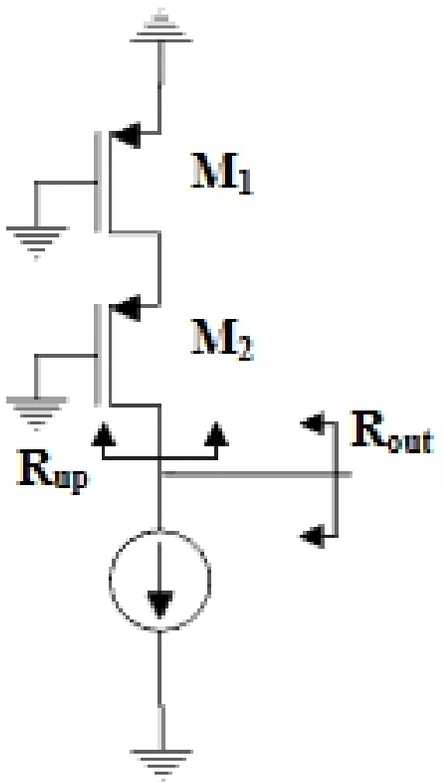

Figure 4. Calculating R_{out}

as follows:

1. v_t causes a current to be generated in M1 through the g_{m1} voltage-dependent current source. More specifically, the current generated has a value of $-g_{m1} \cdot v_t$. This current enters node β from the left, and divides between the right and down branches. One can use the current divider formula to see how the current $-g_{m1} \cdot v_t$ divides between the aforementioned branches.
2. Using the current divider formula, one obtains the following expression for the current flowing through the downward branch from node β,