**University of California at Berkeley**
**College of Engineering**
**Department of Electrical Engineering and Computer Science**

EECS150, Spring 2010

# Discussion 7: SRAM timing, LUT-RAM configurations, Video, Serial, Ethernet

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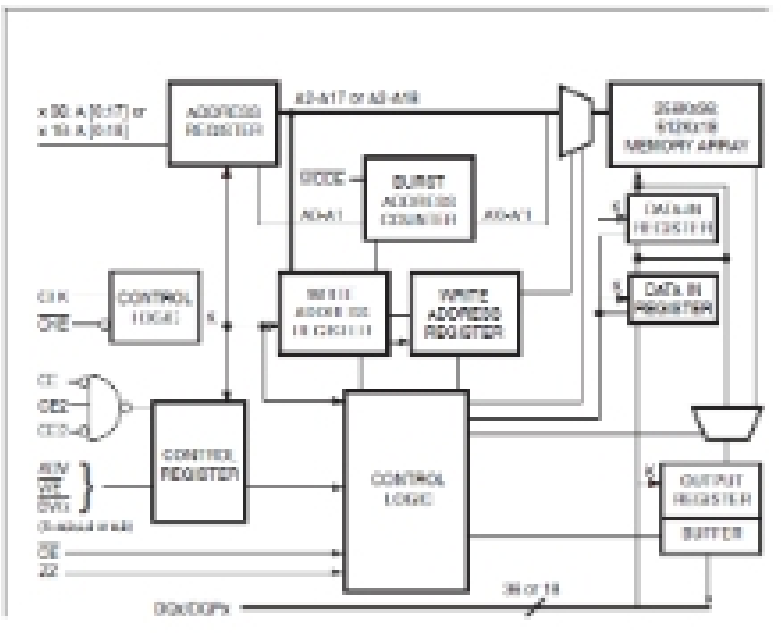
1. Below is a high-level block diagram of the ZBT 9Mb SRAM chip on the XUPv5 boards.




(a) How many cycles does a read require? Draw a timing diagram of a read with signals: clock that is shared by the memory user and the SRAM, the data bus (DQ), address line, and "control signals" (assume this is represented just as a group of signals that can encode READ, WRITE, or NOP command).

(b) Draw a timing diagram of a write, including clock, DQ, address, and "control signals".

2. Refer to the diagram of a SLICEM

(a) Why is RAM64x3SDP an option for a SLICEM memory instead of RAM64x4SDP?

(b) How do you build a single-port 128x1 memory from LUT RAM? Specify SLICEM elements used, and what/how inputs and outputs are used.

(c) dual-port 128x1 memory?

(d) quad-port 32x2 memory? (here quad-port will refer to 1 read/write port and 3 read ports.)

3. Suppose we have a video output device that can display 500 pixels in the horizontal axis, with a horizontal blanking period fixed at $100\mu s$, vertical blanking period fixed at $5ms$, and has a frame rate of 50. The device requires a pixel be sent once every 10ns during non-blanking periods. How many lines does the display have?

4. Suppose a serial line can transmit at 115200 bits/sec. Each byte it transmits must be preceded with a start bit and ended with a stop bit. Suppose ethernet requires a 40-byte header for each packet, and each packet can hold up to 256 bytes of data payload. The ethernet transmits at 1Mbit/sec. What is the overhead for transmission with serial? ethernet? What is the max data rate for each? How long does each take to load a 800x600 image into the framebuffer, where each pixel is 16 bits (state your assumptions; you can start with a simplified model)?