CPSC 614:Graduate Computer Architecture

ILP and Dynamic Execution #3: Examples (Pentium III, Pentium 4, IBM AS/400)

Prof. Lawrence Rauchwerger

Based on Lectures by

Prof. David A. Patterson

UC Berkeley

Review: Dynamic Branch Prediction

- Prediction becoming important part of scalar execution
- Branch History Table: 2 bits for loop accuracy
- Correlation: Recently executed branches correlated with next branch.
  - Either different branches
  - Or different executions of same branches
- Tournament Predictor: more resources to competitive solutions and pick between them
- Branch Target Buffer: include branch address & prediction
- Predicated Execution can reduce number of branches, number of mispredicted branches
- Return address stack for prediction of indirect jump

Review: Limits of ILP

- **1985-2000: 1000X performance**
  - Moore's Law transistors/chip => Moore's Law for Performance/MPU
- **Hennessy: industry been following a roadmap of ideas known in 1985 to exploit Instruction Level Parallelism to get 1.55X/year**
  - Caches, Pipelining, Superscalar, Branch Prediction, Out-of-order execution, …
- **ILP limits: To make performance progress in future need to have explicit parallelism from programmer vs. implicit parallelism of ILP exploited by compiler, HW?**
  - Otherwise drop to old rate of 1.3X per year?
  - Less because of processor-memory performance gap?
- **Impact on you: if you care about performance, better think about explicitly parallel algorithms vs. rely on ILP?**