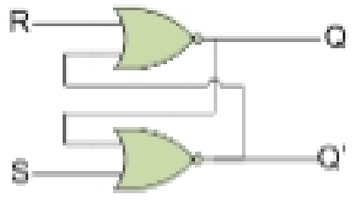
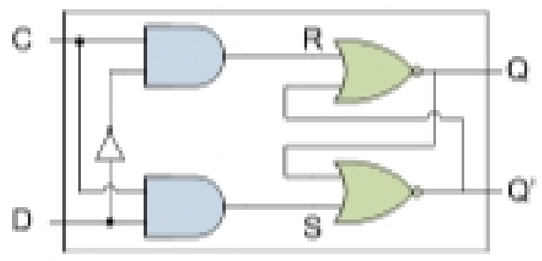
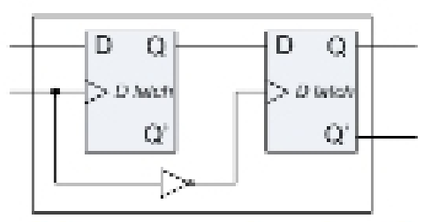
State Elements



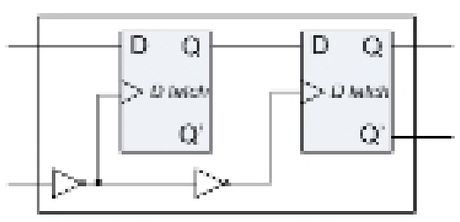
RS latch
R,S control mode (reset, set, storage)
Q,Q' track R and S
R=1, S=1 invalid



D latch
C controls mode (0=latched, 1=transparent)
D is data input ("copied" during transparent)
Signal value triggered: Q,Q' track D when C=1
Guarantees R=1,S=1 can not be done

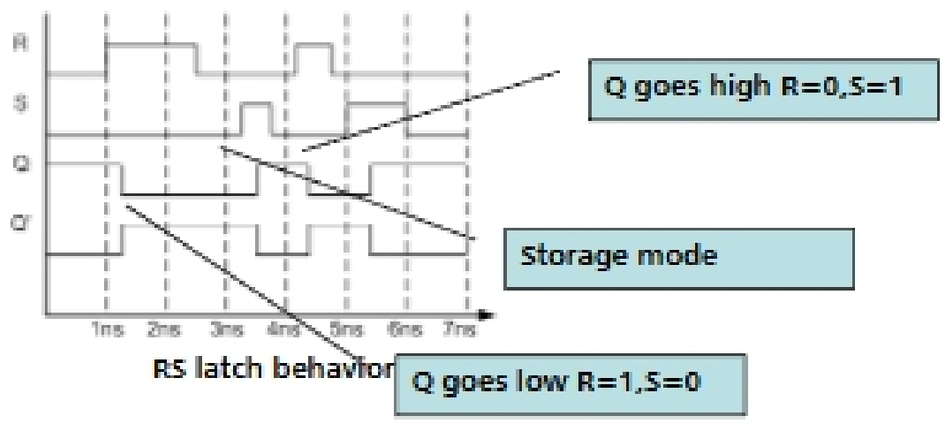


D flip-flop (falling or negative edge triggered)
Two cascaded D latches
C=1 means 1st latch transparent, 2nd latched
C=0 means 1st latch latched, 2nd transparent
Output changes on falling edge (C: 1=>0)

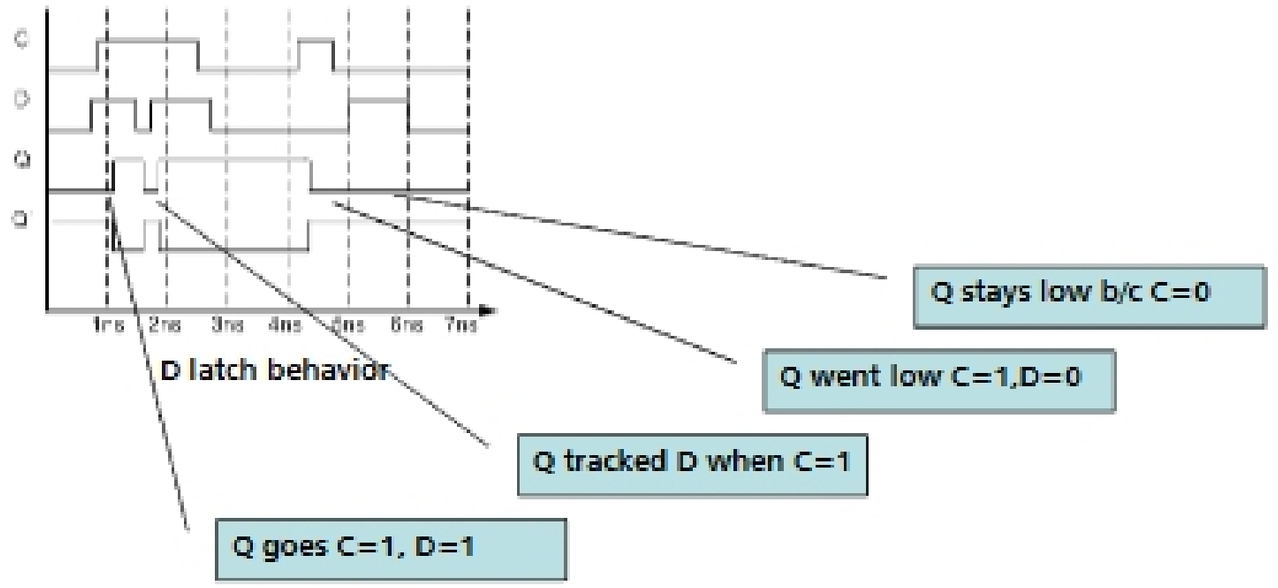


D flip-flop (rising or positive edge triggered)
Same as falling edge triggered
Output changes on rising edge (C: 0=>1)

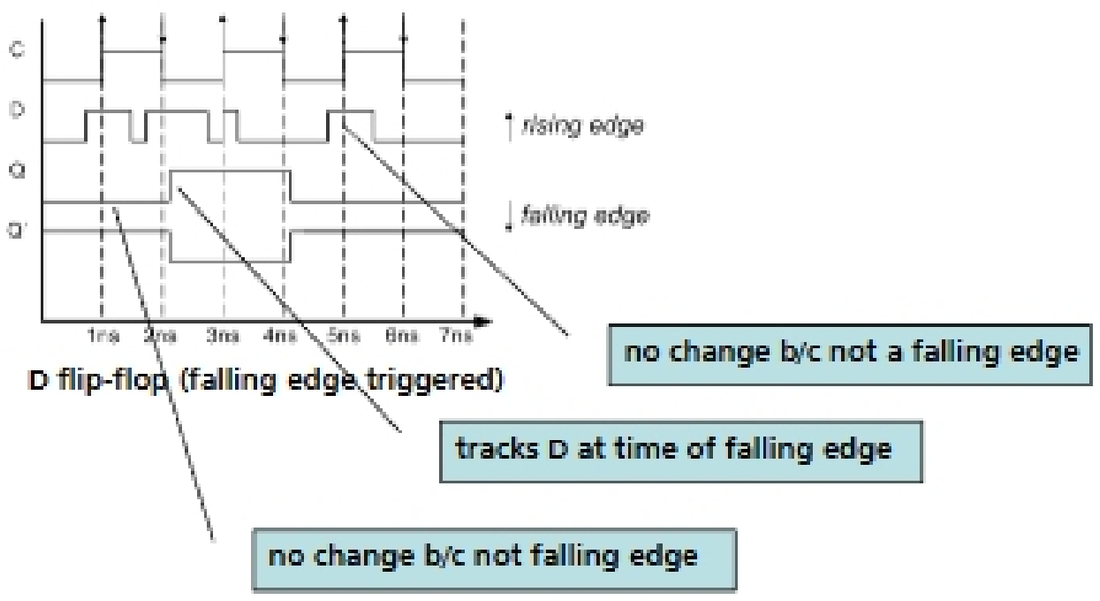
Signaling Behavior



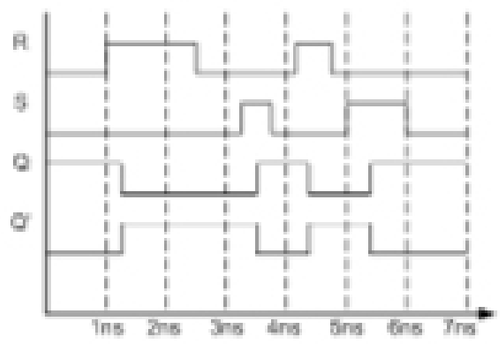
Signaling Behavior



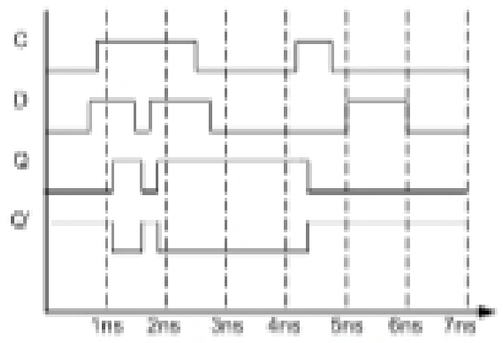
Signaling Behavior



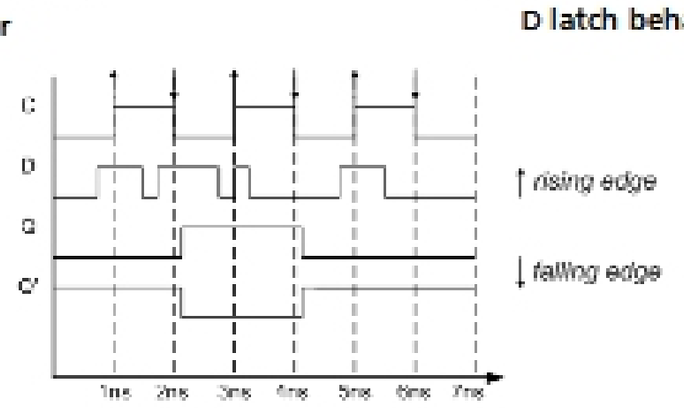
Signaling Behavior



RS latch behavior



D latch behavior



D flip-flop (falling edge triggered)

Example circuits and clocking

- Suppose we want to:
  - 1-bit value A stored in a D flip-flop
  - 1-bit value B stored in a D flip-flop
  - 1-bit value C stored in a D flip-flip
  - Do addition of A and B, producing C
- C = A + B
  - What is the circuit?
  - Need three D flip-flops
  - Need one 1 bit adder