Lecture 33: Embedded System Design

- Design Overview
- Design metrics
  - Cost
  - Performance
  - Power

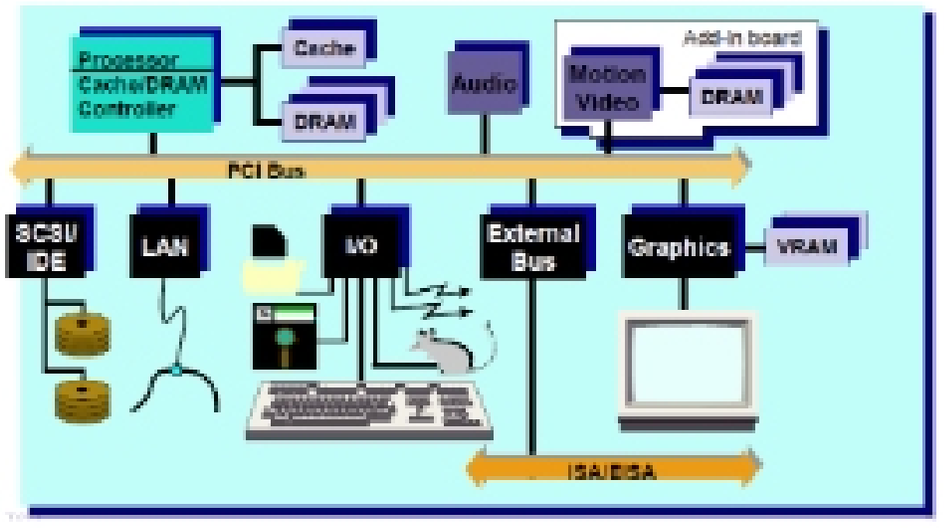
ES Application Classes

Class	Application	Processor	Requirements
Data flow	laser printers, X-terminals, routers, bridges, image processing	R4600, I960,29k, Coldfire, PPC (403, 605)	Processes data and passes it on. High memory bw, high throughput
Interactive video &portable	set-top boxes, videogames, PDAs, portable info appliances	R3900,R4100/4300/4600, ARM6xx/7xx, V851,SH1/2/3	Interactive, low cost, low power, high throughput
Classic embedded	controllers, disk controllers, automotive, industrial control	Piranha, ARM,MIPS, Cores	mix of CPU power, low cost, low power, peripherals

Design is purely application-driven

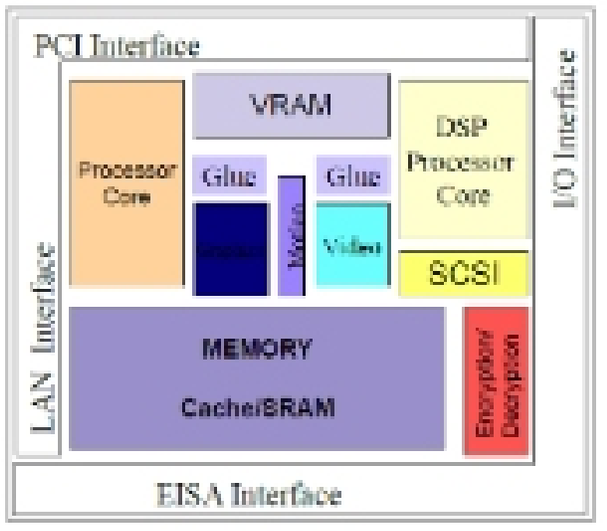
System Architecture: Yesterday

PCB design

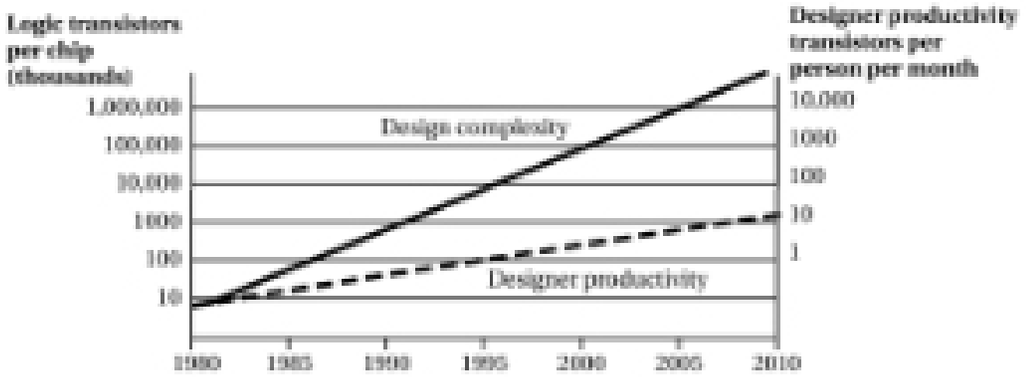


A System Architecture: Today

HW/SW Codesign of a SoC



Design complexity vs. designer productivity



Trends in Embedded Systems

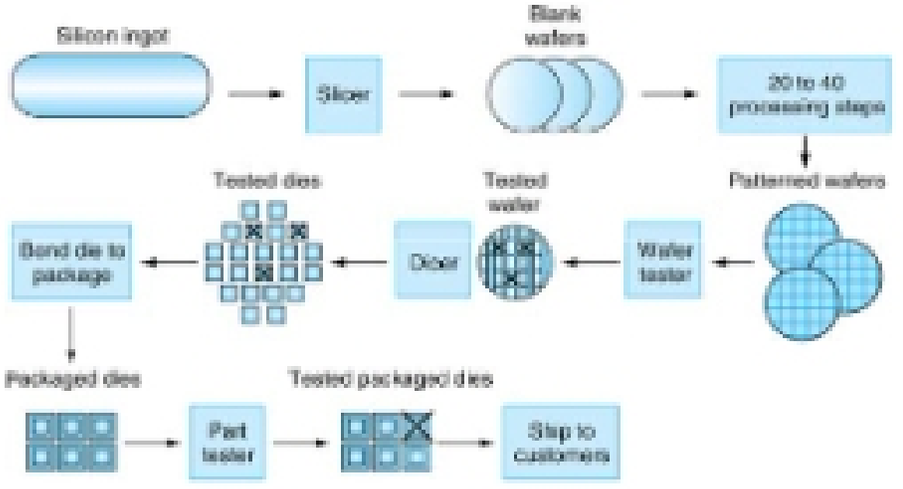
- Increasing code size
  - migration from hand (assembly) coding to high-level languages
- Reuse of hardware and software components
  - processors (micro-controllers, DSPs)
  - software components (drivers)
- Increasing integration and system complexity
  - integration of RF, DSP, network interfaces
  - 32-bit processors, IO processors (I2O)

Structured design and composition methods are essential.

Design goals

- Functional requirements:
  - input/output relations.
- Non-functional requirements:
  - cost, performance, power, etc.

Manufacturing ICs



- **Yield: proportion of working dies per wafer**

IC Manufacturing Cost

$$\text{Cost per die} = \frac{\text{Cost per wafer}}{\text{Dies per wafer} \times \text{Yield}}$$

$$\text{Dies per wafer} \approx \text{Wafer area}/\text{Die area}$$

$$\text{Yield} = \frac{1}{(1+(\text{Defects per area} \times \text{Die area}/2))^2}$$

- Nonlinear relation to area and defect rate
  - Wafer cost and area are fixed
  - Defect rate determined by manufacturing process
  - Die area determined by architecture and circuit design

Increasing Customization Cost

Estimated Cost - 585 M -590 M

Example: Design with 80 M transistors in 100 nm technology

- Top cost drivers
  - Verification (40%)
  - Architecture Design (26%)
  - Embedded Design
    - 1400 man months (SW)
    - 1150 man months (HW)
  - HW/SW integration

IC Cost Analysis

- Cost breakdown:

	ASIC	FPGA
– Design/verification cost	High	Low
– Manufacturing cost	Low	High
– Testing cost	Same	Same
– Maintenance/update cost	Same	Same

- Design and Manufacturing costs must be paid off across all the systems.
  - Small volume uses FPGA
  - Large volume uses ASIC
- Lifetime costs include software and hardware maintenance and upgrades.

Defining Performance

- Which airplane has the best performance?