Lecture 25: Feedback Configurations

- Announcements:
- Design Project Checkpoint:
  - Due Monday, April 25, 11:59 p.m.
  - Send to your TA a spice file for your op amp design that simulates correctly, i.e., that reaches a stable bias point where all transistors are saturated (or linear if an MOS resistor)
  - It doesn't need to meet the project specs, but it should simulate correctly
- Lecture Topics:
  - Power Supply Rejection Ratio (PSRR) – finish w/ an example
  - Advantages of Feedback (revisited)
  - Feedback Configurations
  - Effect of FB on $Z_i$ and $Z_o$
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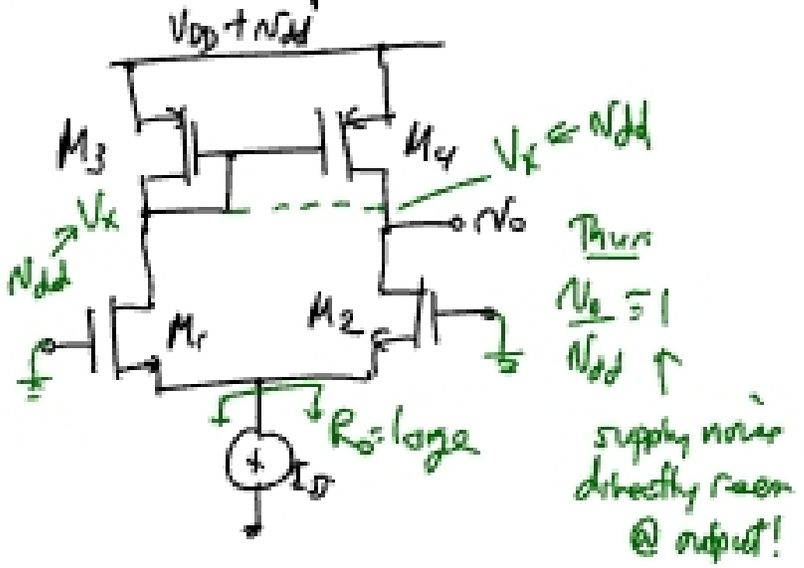
- Last Time: PSRR

Ex. CMOS Diff. Input Stage w/ Current Source Load




Definition: Power Supply Rejection Ratio (PSRR)

$$PSRR \triangleq \frac{\text{Gain from Input to Output}}{\text{Gain from Supply to Output}} = \frac{A_v|_{N_{dd}=0}}{A_{dd}|_{N_i=0}}$$

Thus, for the above example: $PSRR \cong g_{m2}(r_{o2} \| r_{o4})$

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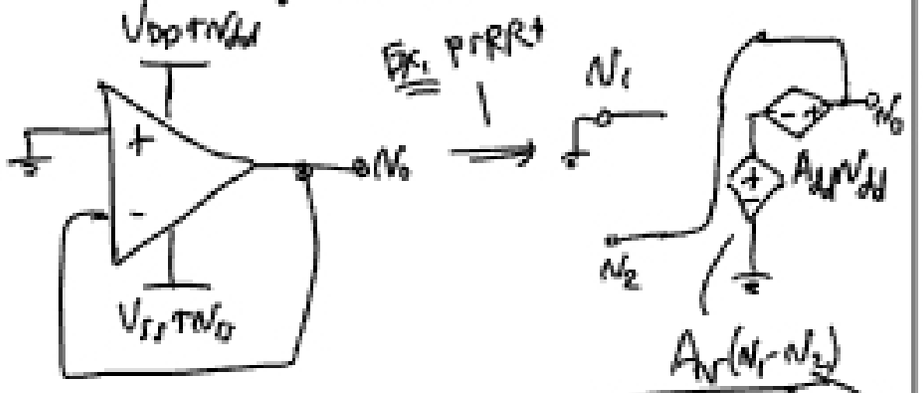
For more complicated ckts, much more is involved.

↳ to make it easier, use a unity gain config.

↳ can also get $PSRR = f(\omega)$




$$N_o = A_v(N_1 - N_2) + A_{dd}N_{dd}$$

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$$-N_o$$

$$N_o(1+A_v) = A_{dd}N_{dd}$$

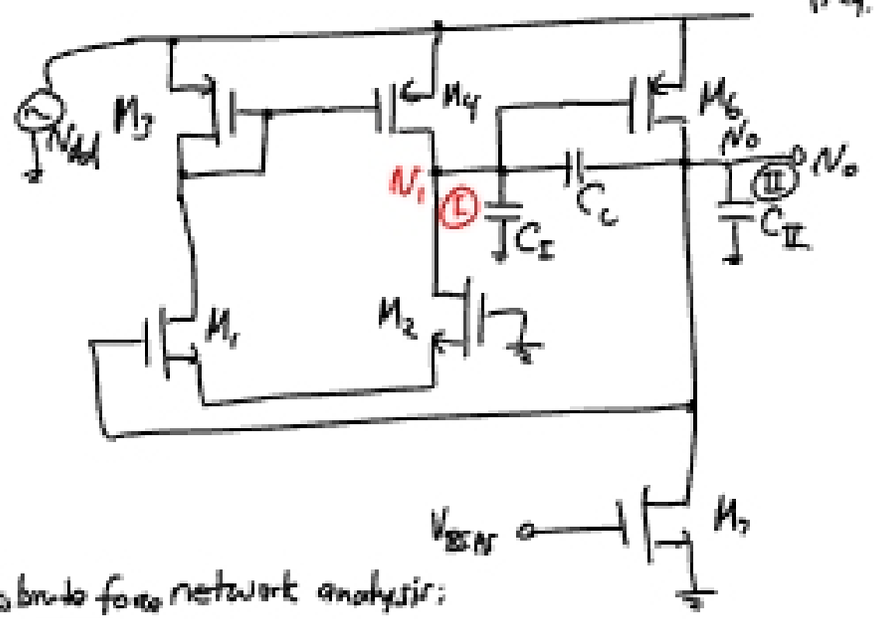
$$\frac{N_o}{N_{dd}} \cdot \frac{A_{dd}}{1+A_v} = \frac{1}{\frac{1}{A_{dd}} + \frac{A_v}{A_{dd}}} \approx$$

$$PSRR+ = \frac{N_{dd}}{N_o}$$

$$\frac{1}{PSRR+} = \frac{N_o}{N_{dd}}$$

## Two-Stage Op Amp PSRR+

Want PSRR+ = f(ω) ↑ freq.




Do brute force network analysis:

KCL①: $G_I V_{dd} = (G_I + sC_c + sC_1)V_1 - (g_{m2} + sC_c)V_o$

KCL②: $(g_{mII} + g_{ds6})V_{dd} = (g_{m2} - sC_c)V_1 + (G_{II} + sC_c + sC_{II})V_o$

$G_I = g_{ds1} + g_{ds4} = g_{ds2} + g_{ds4}$
$G_{II} = g_{ds6} + g_{ds7}$
$g_{mI} = g_{m1} = g_{m2}$
$g_{mII} = g_{m6}$

$[g_{ds} = \frac{1}{r_o}]$ for saturated device.

Get: $\left(\frac{V_{dd}}{V_o}\right)_{closed\text{-}loop} = \frac{N(s)}{D(s)}$ : ( ) polynomials

math & manipulating

↳ then use: $N(s) = 1 + \left(\frac{s}{z_1} + \frac{s}{z_2}\right) + \frac{s^2}{z_1 z_2} \approx 1 + \frac{s}{z_1} + \frac{s^2}{z_1 z_2}$

$$PSRR+ = A_{Vo}^{+}\left[\frac{(1+\frac{s}{GB})(1+\frac{s}{|p_2|})}{(1+\frac{s}{GB/A_{Vo}^{+}})}\right]$$

where GB = Gain BW product = $\frac{g_{mI}}{C_c}$

$A_{Vo}^{+}$ = DC PSRR+ = $\frac{g_{mI}g_{mII}}{G_I g_{ds6}}$

$|p_2| = \frac{g_{mII}}{C_{II}}$ $\omega_p^{+} = \frac{GB}{A_{Vo}^{+}}$

To maximize PSRR+: (@dc) decrease $g_{ds6}$, raise $g_{mII}$

PSRR-: $A_{Vo}^{-}\left[\frac{(1+\frac{s}{GB})(1+\frac{s}{|p_2|})}{(1+\frac{s}{\omega_p^{-}})}\right]$

where $A_{Vo}^{-} = \frac{g_{mI}g_{mII}}{G_I g_{ds7}}$

$GB = \frac{g_{mI}}{C_c}$ $\omega_p^{-} = \frac{G_I}{C_o + C_I} \approx \frac{G_I}{C_c}$

$|p_2| = \frac{g_{mII}}{C_{II}}$

To maximize PSRR-: ① decrease $g_{ds7}$
② increase $g_{mII} = g_{m6}$

Remarks:

① Since often $g_{mn7} < g_{m56}$ → often $PSRR^- > PSRR^+$ (@ dc)

② $$\frac{\omega_p^-}{\omega_p^+} \cdot \frac{\cancel{g_{m3}/C_L}}{\cancel{C_1 g_{m56}}/\cancel{g_{m8}C_L}} = \frac{g_{mIII}}{g_{m56}}$$ → that's quite large

$\therefore \omega_p^- \gg \omega_p^+$

Thus, for an NMOS input op amp, $PSRR^-$ is often better than $PSRR^+$. → in design, need to worry more about $PSRR^+$!

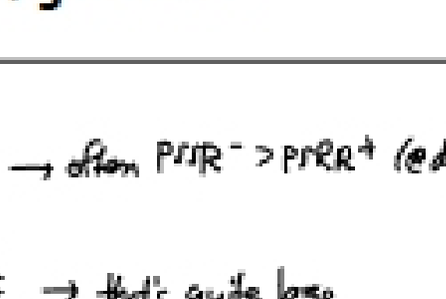
③ Some methods for reducing PSRR:

(i) Use bulk-based zero-cancellation in the compensation loop.

(ii) Use cascode circuitry, or balanced circuit topologies.

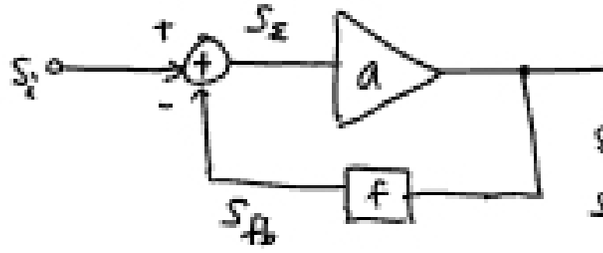
(iii) Supply-independent biasing.

(iv) Design strategies to minimize parasitic capacitive feedthrough.




**Feedback**

⇒ we know this:




$S_o = a S_\varepsilon$

$S_\varepsilon = S_i - f S_o$

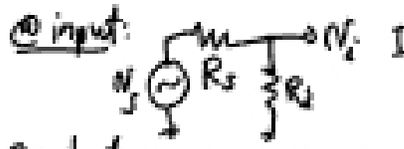
$$\frac{S_o}{S_i} = \frac{a}{1+af} = A$$

Benefits of Negative FB:

① Stabilizes the gain of the amp against parameter changes & active device variations

② Modifies $R_i$ and $R_o$ → basically improves their values according to the type of amplifier implemented

e.g., voltage amp: $R_i$: large, $R_o$: small

@ input: 

If $R_i$: large, $V_i \propto V_s$. ($R_i \gg R_s$)

@ output: 

If $R_o$: small, $V_o \propto V_o'$. ($R_o \ll R_L$)

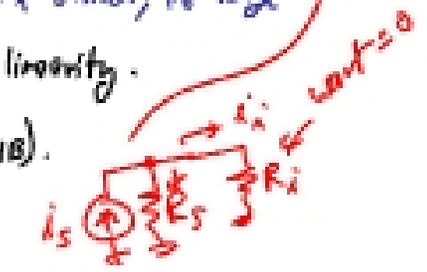
current-to-voltage amp: $R_i$: small, $R_o$: small

voltage-to-current amp: $R_i$: large, $R_o$: large

current-to-current amp: $R_i$: small, $R_o$: large

③ Reduces distortion; improves linearity.

④ Increases bandwidth (ω.3dB).




Disadvantages of Neg. FB:

① Gain is reduced → reduction factor ~ equal to the amount of gain stabilization, distortion reduction, etc...

Solution: Add more stages of gain → but this adds cost & power...

② Feedback causes stability problems (if not compensated properly)