CPSC 614:Graduate Computer Architecture

Memory Technology

Prof. Lawrence Rauchwerger

Based on lectures by

Prof. David Culler

Prof. David Patterson

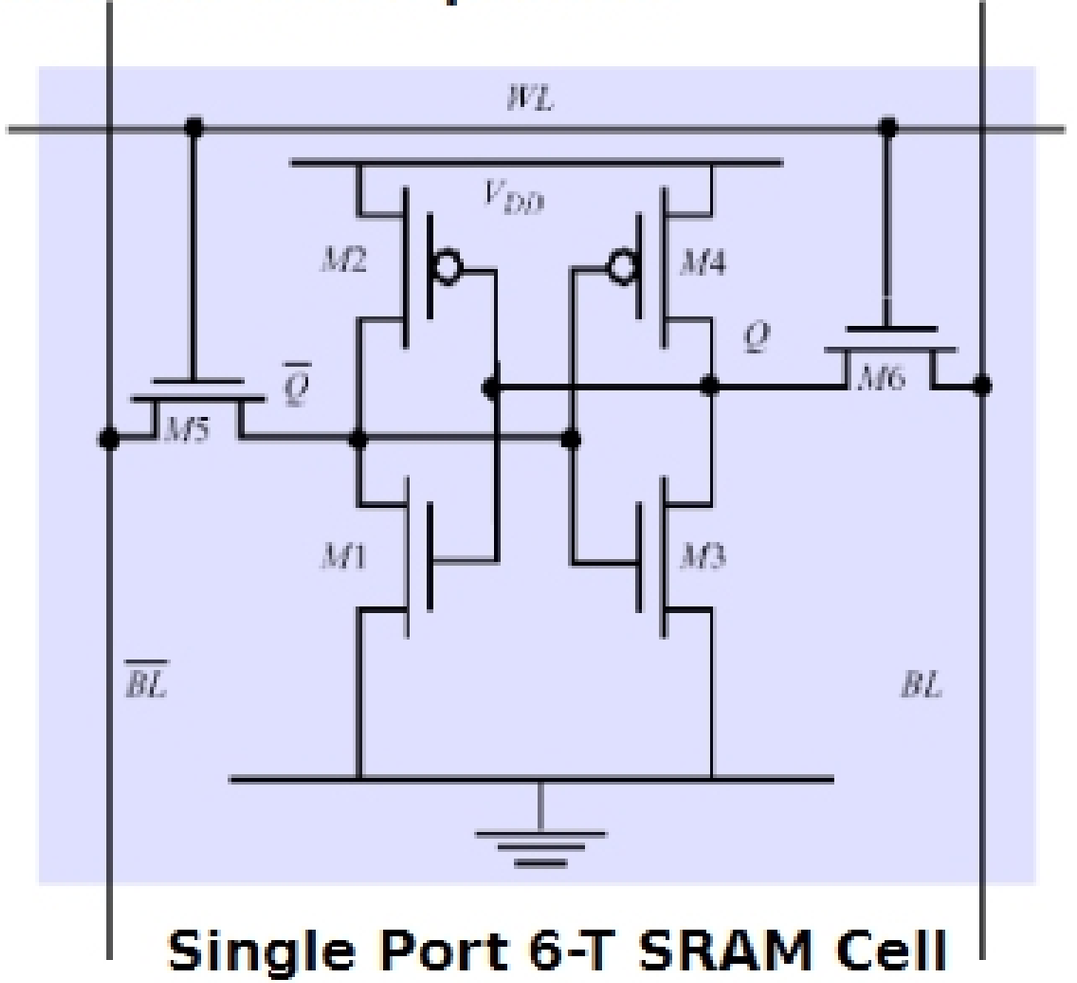
UC Berkeley

Main Memory Background

- Random Access Memory (vs. Serial Access Memory)
- Different flavors at different levels
  - Physical Makeup (CMOS, DRAM)
  - Low Level Architectures (FPM,EDO,BEDO,SDRAM)
- Cache uses *SRAM*: Static Random Access Memory
  - No refresh (6 transistors/bit vs. 1 transistor
    Size: DRAM/SRAM *4-8*,
    Cost/Cycle time: SRAM/DRAM *8-16*
- Main Memory is *DRAM*: Dynamic Random Access Memory
  - Dynamic since needs to be refreshed periodically (8 ms, 1% time)
  - Addresses divided into 2 halves (Memory as a 2D matrix):
    - » *RAS* or *Row Access Strobe*
    - » *CAS* or *Column Access Strobe*

Static RAM (SRAM)

- **Six transistors in cross connected fashion**
  - Provides regular AND inverted outputs
  - Implemented in CMOS process



Single Port 6-T SRAM Cell