

UNIVERSITY OF CALIFORNIA AT BERKELEY
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Design Problem 1
(Due 2/12/04)

EECS 140
Spring 2004

1. Design Specification

You are asked to design a CMOS amplifier with a gain of at least 500, while driving a resistive load, shown in Figure 1. The available circuit components are NMOS transistors, PMOS transistors or resistors. Ideal sources can only be used to generate the supply voltages, not to generate bias currents or voltages. The design specifications are as following,

- $L_{min} = 0.13\mu\text{m}$, $W_{min,nmos} = 0.15\mu\text{m}$, $W_{min,pmos} = 0.15\mu\text{m}$;
- $V_{dd} = 1.2\text{ V}$, $V_{ss} = 0\text{ V}$;
- $R_L = 50\Omega$;
- V_{out} biasing point $0.5\sim 0.7\text{ V}$;
- V_{in} biasing point (V_{ic}) $0.35\sim 0.85\text{ V}$;
- Total gain $V_{out}/V_{id} \geq 500$.

The design goal is to minimize the following figure of merit ($\text{Watts} \cdot \mu\text{m}^2$),

$$FOM = \text{Power} \cdot \text{Area}$$

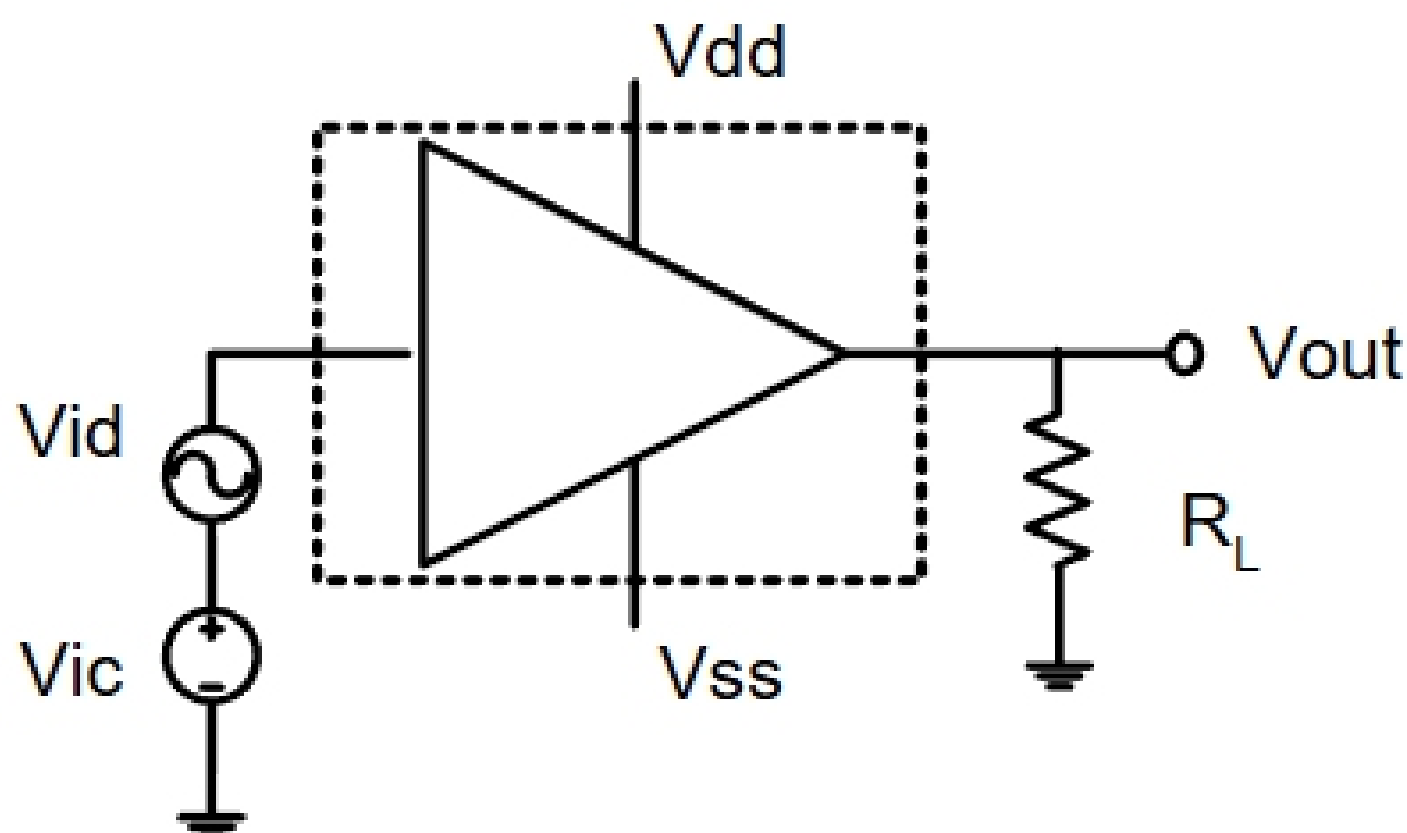


Figure 1

2. Area Calculation

Calculate the area by adding up the gate area ($W \cdot L$) of all the transistors and the area of the resistors. For the transistors, the minimum L is $0.13 \mu\text{m}$ and the minimum W is $0.15 \mu\text{m}$. For the resistors, the minimum W and L are $0.5 \mu\text{m}$; the sheet resistance is $250\Omega/\text{square}$. You are allowed to tie the bulk of any transistor to the source instead of to the positive or negative supply, but at the cost of an area penalty. If you choose to tie the bulk to the source, the area of the transistor should be doubled.

3. Device Models

http://bwrc.eecs.berkeley.edu/classes/ee140/dp/model_ee140.sp

The device models are encapsulated in a sub-circuit; use:

```
x1 d g s b nmos w=10u l=0.13u
```

```
x2 d g s b pmos w=10u l=0.13u
```

to instantiate an NMOS and a PMOS transistor respectively (you have to use the prefix 'x' instead of 'm'). The reason for using a subcircuit is to allow λ to decrease with increasing transistor length. The output resistance parameter λ will stay the same as before for minimum length transistors ($L_{\text{min}}=0.13\mu\text{m}$), but will decrease with increasing L (drawn L , not effective L). Since the output resistance is proportional to $1/\lambda$, the output resistance increases with increasing L . Since we are using level-2 device model, it is worthwhile to calculate level-1 parameters of the device model for your hand calculations. (Ref: problem 1 of HW1, extracting K' , λ , γ , etc.)

4. Run testbench

Perform dc operation point and small-signal transfer function analysis.

Usage: put `testbench_dp1.sp`, `model_ee140.sp`, `circuit.sp` in the same directory and run `'hspice testbench_dp1.sp -o testbench_dp1'`.

5. What to include in your report

http://bwrc.eecs.berkeley.edu/classes/ee140/dp/guidelines_dp1.pdf

6. Grading

100 points total:

45 points for conciseness and clearness of the report

45 points for meeting the specifications

10 points for how well FOM is minimized