EGR 270
Fundamentals of Computer Engineering
File: N270L7

Lab # 7

Sequential Circuit Design using FPGAs

Lab Format

- This is a **Individual Lab** so each student must design and test their own circuits.
- Each student must complete the Preliminary Work Section **before** lab begins. Preliminary Work will be checked in lab and will be part of the lab report grade.
- Each student must submit his or her own lab report.
- Lab reports will not be accepted until all required circuits have been demonstrated to the instructor.

A. Objective

The objective of this laboratory is to introduce students to the use of sequential circuit design using Field Programmable Gate Arrays (FPGAs). Each student will design a sequential circuit using the State Diagram Wizard in Aldec Active HDL. The design will be simulated in Aldec Active HDL and the corresponding VHDL file will be combined with other VHDL files to provide for a 1Hz clock input and an output display on a 7-segment display. The complete design will be synthesized using Xilinx ISE 11 and implemented into a Spartan 3E FPGA on the BASYS2 FPGA board where the student can test the design for proper operations.

B. Materials

Aldec Active-HDL Software
Xilinx ISE 11 Software
Digilent Adept Software
BASYS2 FPGA Board

C. Reference

Refer to the following items (available on the course Bb site):

- ***"Sequential Logic Circuits using Aldec Active-HDL 8.1 and Xilinx ISE 11"***
- ***"Combinational Logic Circuits using Aldec Active-HDL 8.1 and Xilinx ISE 11"***
- Digilent BASYS2 FPGA Board Reference Manual

D. Introduction

Although we will make use of the State Diagram Wizard in Aldec Active-HDL, we could also enter a design for a sequential circuit directly in VHDL. One method for doing this is to write state equations. In order to give the student an appreciation of the design work that would be required by hand and the complexity of the circuit to be implemented into the FPGA, students will be required to perform a hand design as well.

Sequential circuit design using state equations

Several design methods are available for designing synchronous sequential circuits, including the excitation table method, design by state equations, and design using the "one-hot" method. Since the D flip-flop is an essential part of the FPGA, we will focus on the ***state equation method*** which is well suited for D flip-flops.
The general form of the state equation for a D flip-flop is:

$$Q(t+1) = D$$

So the input for each D flip-flop is si[illegible] by finding an expression for the next state for that flip-flop.

Example: Design a 4-bit counter using D flip-flops and the state equation method.

A 4-bit counter, also called a modulo-16 counter, counts in the sequence 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 and repeats. The state diagram is shown in Figure 1 below.

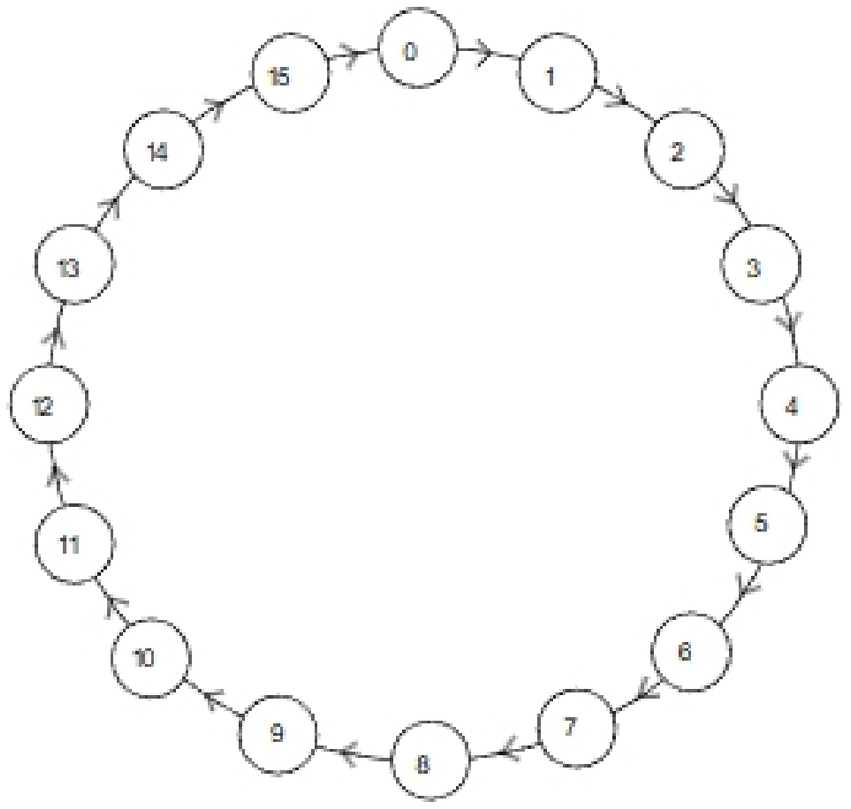

Figure 1: State diagram for a 4-bit counter

The corresponding state table is shown in Figure 2 below. Note that the state is shown in decimal form in the state diagram, whereas it is shown in binary form in the state table with bit D as the MSB.

Present State				Next State			
D	**C**	**B**	**A**	**D**	**C**	**B**	**A**
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

Figure 2: State table for a 4-bit counter

The characteristic equation for a D flip-flop is very simple: **Q(t + 1) = D.**
So the expression for the next state is simply connected to the D input on the flip-flop. Expressions for the next state for each of the four flip-flops is determined using Karnaugh maps shown in Figure 3 below.

D(t + 1)

DC \ BA	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	1	1	0	1
10	1	1	1	1

C(t + 1)

DC \ BA	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	1	1	0	1
10	0	0	1	0

B(t + 1)

DC \ BA	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

A(t + 1)

DC \ BA	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	1	0	0	1
10	1	0	0	1

Figure 3: Karnaugh maps for the state equations for the 4-bit counter

Minimal SOP expressions for each output yield the state equations shown below in Figure 4:

$$D(t+1) = D \bullet \overline{C} + D \bullet \overline{B} + D \bullet \overline{A} + \overline{D} \bullet C \bullet B \bullet A$$
$$C(t+1) = C \bullet \overline{B} + C \bullet \overline{A} + \overline{C} \bullet B \bullet A$$
$$B(t+1) = B \bullet \overline{A} + \overline{B} \bullet A$$
$$A(t+1) = \overline{A}$$

Figure 4: State equations for the 4-bit counter

The state equations above are implemented in the circuit shown below in Figure 5.

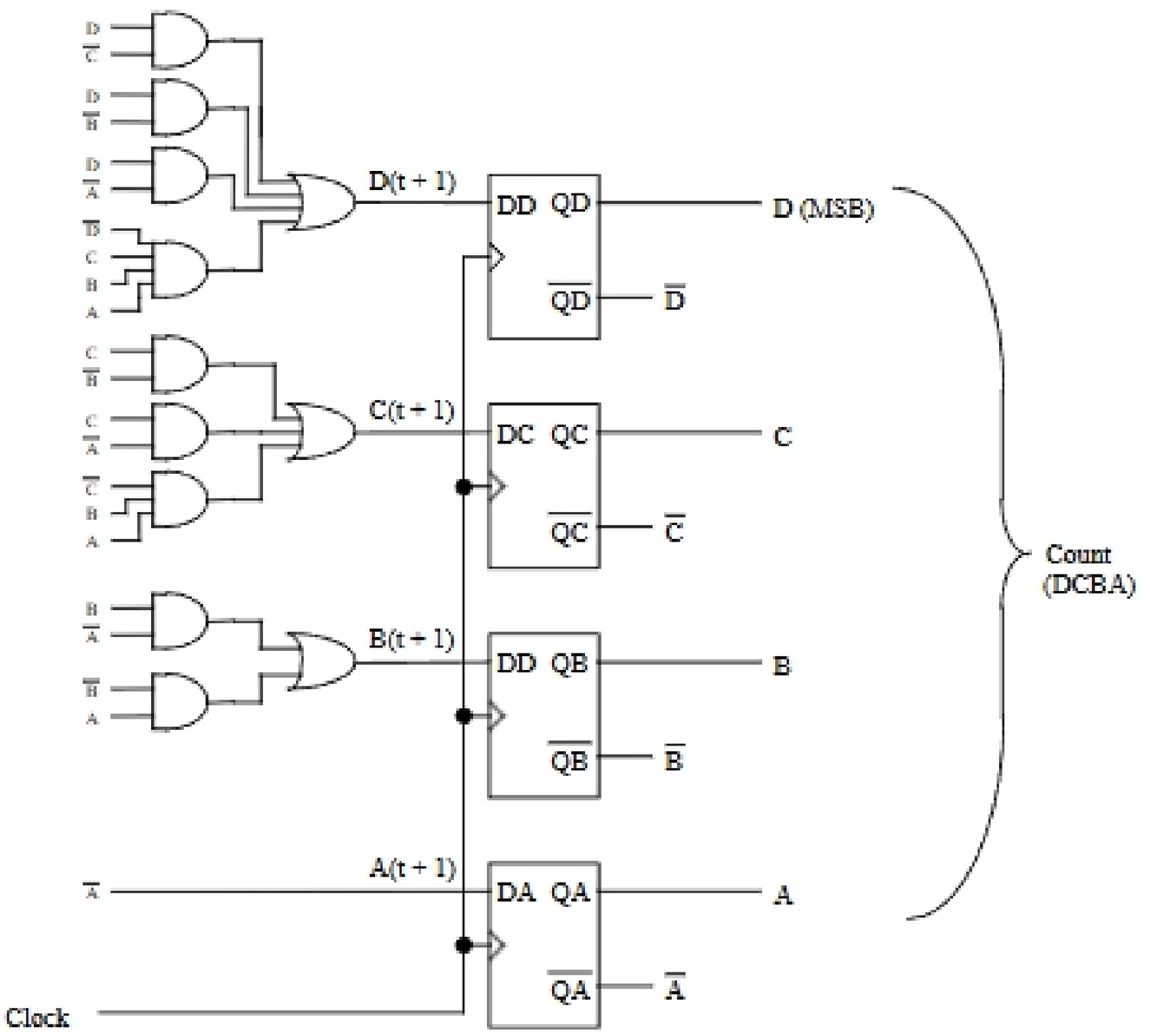

Figure 5: Logic Diagram for the 4-bit counter

E. Preliminary Work