ORCA FPGAs

ORCA® Series 3C and 3T Field-Programmable Gate Arrays

Features

- High-performance, cost-effective, 0.35 µm (OR3C) and 0.3 µm (OR3T) 4-level metal technology. (4- or 5-input look-up table delay of 1.1 ns with -7 speed grade in 0.3 µm).
- Same basic architecture as lower-voltage, advanced process technology Series 3 architectures. (See *ORCA* Series 3L FPGA documentation.)
- Up to 186,000 usable gates.
- Up to 452 user I/Os. (OR3Txxx I/Os are 5 V tolerant to allow interconnection to both 3.3 V and 5 V devices, selectable on a per-pin basis.)
- Pin selectable I/O clamping diodes provide 5 V or 3.3 V PCI compliance and 5 V tolerance on OR3Txxx devices.
- Twin-quad programmable function unit (PFU) architecture with eight 16-bit look-up tables (LUTs) per PFU, organized in two nibbles for use in nibble- or byte-wide functions. Allows for mixed arithmetic and logic functions in a single PFU.
- Nine user registers per PFU, one following each LUT, plus one extra. All have programmable clock enable and local set/reset, plus a global set/reset that can be disabled per PFU.
- Flexible input structure (FINS) of the PFUs provides a routability enhancement for LUTs with shared inputs and the logic flexibility of LUTs with independent inputs.
- Fast-carry logic and routing to adjacent PFUs for nibble-, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Softwired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU for up to 40% speed improvement.
- Supplemental logic and interconnect cell (SLIC) provides 3-statable buffers, up to 10-bit decoder, and *PAL**-like AND-OR with optional INVERT in each programmable logic cell (PLC), with over 50% speed improvement typical.
- Abundant hierarchical routing resources based on routing two data nibbles and two control lines per set provide for faster place and route implementations and less routing delay.
- TTL or CMOS input levels programmable per pin for the OR3Cxx (5.0 V) devices.
- Individually programmable drive capability: 12 mA sink/6 mA source or 6 mA sink/3 mA source.
- Built-in boundary scan (*IEEE*†1149.1 JTAG) and TS_ALL testability function to 3-state all I/O pins.
- Enhanced system clock routing for low skew, high-speed clocks originating on-chip or at any I/O.
- Up to four ExpressCLK inputs allow extremely fast clocking of signals on- and off-chip plus access to internal general clock routing.
- StopCLK feature to glitchlessly stop/start ExpressCLKs independently by user command.
- Programmable I/O (PIO) has:
  - — Fast-capture input latch and input flip-flop (FF) latch for reduced input setup time and zero hold time.
  - — Capability to (de)multiplex I/O signals.
  - — Fast access to SLIC for decodes and *PAL*-like functions.
  - — Output FF and two-signal function generator to reduce CLK to output propagation delay.
  - — Fast open-drain dive capability.
  - — Capability to register 3-state enable signal.
- Baseline FPGA family used in Series 3+ FPSCs (field programmable system chips) which combine FPGA logic and standard cell logic on one device.

* *PAL* is a trademark of Advanced Micro Devices, Inc.

† *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

ORCA® FPGA Resources

Table 1. *ORCA* Series 3 (3C and 3T) FPGAs

Device	System Gates‡	LUTs	Registers	Max User RAM	User I/Os	Array Size	Process Technology
OR3T20	36K	1152	1872	18K	196	12 x 12	0.3 µm/4 LM
OR3T30	48K	1568	2436	25K	228	14 x 14	0.3 µm/4 LM
OR3C/3T55	80K	2592	3780	42K	292	18 x 18	0.3 µm/4 LM
OR3C/3T80	116K	3872	5412	62K	356	22 x 22	0.3 µm/4 LM
OR3T125	186K	6272	8400	100K	452	28 x 28	0.3 µm/4 LM

‡The system gate counts range from a logic-only gate count to a gate count assuming 30% of the PFUs/SLICs being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates per PFU/SLIC), including 12 gates per LUT/FF pair (eight per PFU), and 12 gates per SLIC/FF pair (one per PFU). Each of the four PIOs per PIC is counted as 16 gates (two FFs, fast-capture latch, output logic, CLK drivers, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU.