EECS150 - Digital Design

Lecture 20 - Finite State Machines 2

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Outline

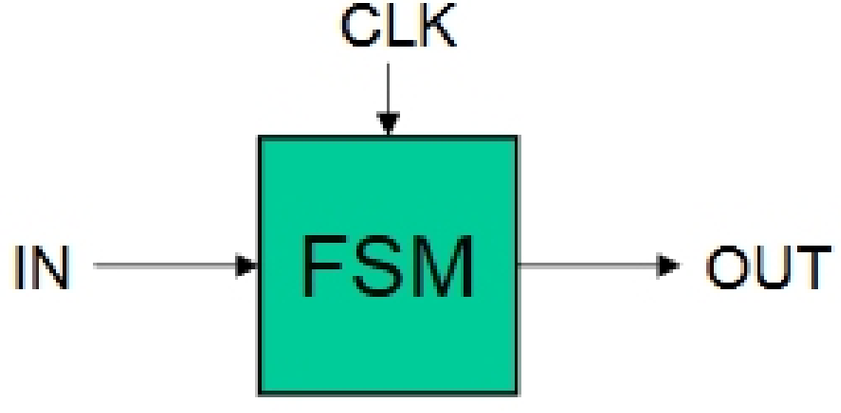
- Moore versus Mealy style state machines.
- FSM optimization
  - State Reduction
  - State Assignment

Finite State Machines

- **Example: Edge Detector**

  Bit are received one at a time (one per cycle),
  such as: 000111010 ⟶ *time*

  Design a circuit that asserts its output for one cycle when the input bit stream changes from 0 to 1.



  Try two different solutions.