

EGR 270 Lab Information

Lab Policies

- The lab grade makes up 25% of the course grade for EGR 270.
- Each lab session will begin with a lecture by the instructor on the following lab. Attendance for the lectures is critical as new material is introduced in many of the labs.
- Students may work alone or with a partner on some of the labs. However, some labs require the design and/or implementation of customized circuits (on the EmplID, for example), so students must work alone on these labs.
- Each student must submit their own lab report for each lab.
- Lab reports are due on the date of the next lab. For example, Lab Report #2 is due on the day the class will be performing Lab #3.
- The key to each lab is proper verification of circuit operation. Therefore,

Tentative Schedule

Date	Topic
Jan 8	No class
Jan 15	Introduction to lab equipment, course procedures, etc.
Jan 22	Lab #1: Introduction to Logic Circuits
Jan 29	Lab #2: Characteristics of TTL gates
Feb 5	Test 1 or Lab #2 continued (if necessary)
Feb 12	Test 1 or Lab #2 continued (if necessary)
Feb 19	Lab #3: Combinational Logic Circuits
Feb 26	Lab #4: 7-segment displays, decoders, and multiplexers
Mar 4	Lab #5 VHDL Combinational Logic Circuit
Mar 11	TCC Closed – Spring Break
Mar 18	Test 2 or Lab #5 continued (if necessary)
Mar 25	Test 2 or Lab #5 continued (if necessary)
Apr 1	Lab #6: Sequential Counters
Apr 8	Lab #7: VHDL Sequential Logic Circuit
Apr 15	Lab #8: Assembly language/MicroStamp11
Apr 22	Lab #8 continued (if necessary)