



Chapter 11

Verilog HDL

Application-Specific Integrated Circuits

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Verilog HDL

- Verilog is an alternative hardware description language to VHDL developed by Gateway Design Automation
- Cadence purchased Gateway and placed Verilog in the public domain (Open Verilog International - OVI)
- An IEEE standard version of Verilog was developed in 1995 [IEEE Std. 1364-1995 Verilog LRM]
- In spite of this standardization, many flavors (usually vendor specific) of Verilog still persist
- Verilog syntax is much like C
- Verilog use is generally most prevalent on the West Coast (Silicon Valley)
- Most high-end commercial simulators support both VHDL and Verilog and you may receive IP blocks for your designs in Verilog which you will be expected to be able to work with
- OVI and VHDL International have recently merged further indicating a dual (or multi) language environment will become more prevalent



Verilog Identifiers

- Identifiers (names of variables, wires, modules, etc.) can contain any sequence of letters, numbers, '\$', or '_'
- The first character of an identifier must be a letter or underscore
- Verilog identifiers are case sensitive

```
reg legal_identifier, two__underscores;  
reg _OK, OK_, OK_$, CASE_SENSITIVE, case_sensitive;
```