Homework 4 – Timers/Counters

Assigned Date: Wednesday, October 29, 2014

Due Date: Wednesday, November 12, 2014

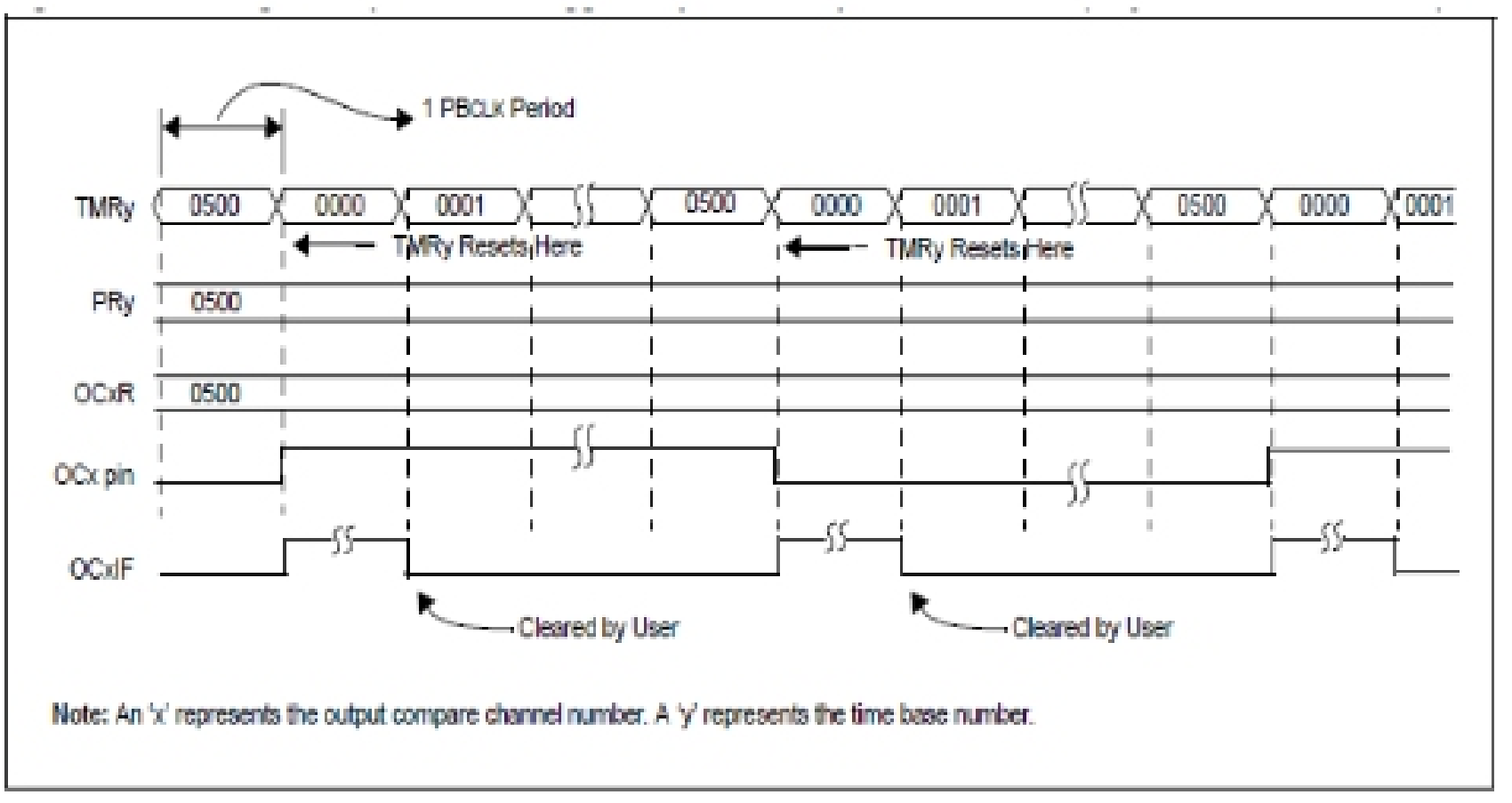
Weight: 60 pts

Problem 1 (10 points total)

Let's say that we take our peripheral clock (80 MHz) and divide it by 128. We call the divided frequency clock Tn_{clk} and use this clock to control the incrementing of our 16-bit timer/counter. Let's further add that we toggle the signal produced by our timer/counter every time the 16-bit timer matches our period register value of 0x003F. What is the resulting frequency of our signal obtained (show the result to the hundredths place)? Show all calculations!

Problem 2 (10 points total)

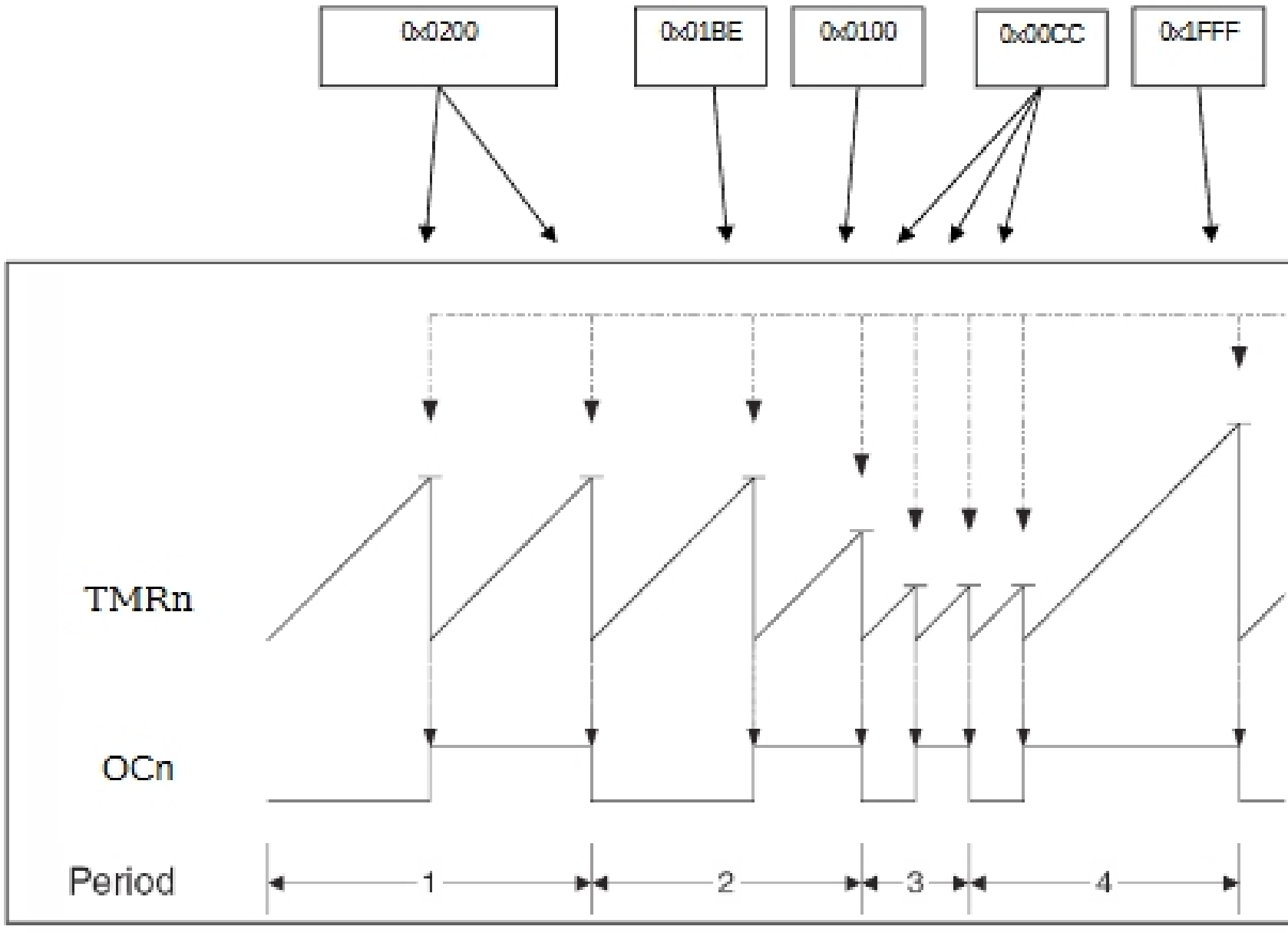
Provided the following diagram and the fact PR_y and OCxR remain constant, what is the resulting frequency of the OCx signal (show the result to the hundredths place)? What is the duty cycle of OCx (show the result to the hundredths place)? NOTE: the diagram shows the Output Compare Module operating in "toggle output on compare match", not PWM mode. This mode operates so that when the value in TMRy matches the value in OCxR, the output signal is toggled. Also, assume TMRy is incrementing every 60 microseconds.



p. 10 of Output Compare Reference

Problem 3 (30 points total)

For each of the four periods shown below for the OCn signal, (a) calculate the period in seconds, (b) calculate the corresponding frequency, and (c) calculate the duty cycle as a percentage. Assume that TMRn is incremented at a frequency of clk_{Tn} = 10 MHz/32. The diagram is not to scale.



Problem 4 (10 points total)

Provide a timing diagram which illustrates an OCx PWM signal with 90% duty cycle. You need to also provide values for TMR_y, PR_y, and OCxR in the diagram.