

# Lecture 3: Directory Protocol Implementations

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- Topics: coherence vs. msg-passing, corner cases in directory protocols

# Future Scalable Designs

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- Intel's Single Cloud Computer (SCC): an example prototype
- No support for hardware cache coherence
- Programmer can write shared-memory apps by marking pages as uncacheable or L1-cacheable, but forcing memory flushes to propagate results
- Primarily intended for message-passing apps
- Each core runs a version of Linux
- Barrelfish-like OSes will likely soon be mainstream

# Scalable Cache Coherence

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- Will future many-core chips forego hardware cache coherence in favor of message-passing or sw-managed cache coherence?
- It's the classic programmer-effort vs. hw-effort trade-off ... traditionally, hardware has won (e.g. ILP extraction)
- Two questions worth answering: will motivated programmers prefer message-passing?, is scalable hw cache coherence do-able?