

CS 152 Computer Architecture

Final Project Report

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Prof. Kubiawicz

Section: 2-4 pm Wednesday
TA: Ed Liao

Team members:

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Abstract:

We implemented a deep-pipelined processor with seven stages, along with a branch predictor, separate instruction and data cache, and stream buffer. Based on the original 5-staged pipeline, we divided the instruction fetch stage into two, the same as the execution stage. At the first fetch stage, the PC is read from the instruction cache while the branch decision is predicted at the second fetch stage. Since the ALU is the function unit that accounts for the worst delay time (15ns), to achieve optimal performance, we broke it down into two 16-bit adders. Each adder is paired with a logical unit and is placed on different execution stages. We also added a branch predictor on the second stage. With this implementation, our pipelined processor can sustained a cycle time of 22.5ns, with the ideal memory system.

To optimize our memory system, we implemented two cache subsystems, one for the data and the other for the instruction. Furthermore, due to the frequency of sequential memory accesses to the instruction cache, we attached a stream buffer to it. And finally, the performance metrics that we used for the cache are the hit time and miss penalty. The hit time for both data and instruction caches is 7ns. The miss penalty for the data cache is estimated as 124.5ns while that for the instruction cache is 422ns, based on the result from running the mystery program with the ideal memory.

Division of Labor:

Project Design Areas	Team Member(s) Involved
Processor datapath, and controllers	Sonkai Lao, Lin Zhou
Cache system, controllers, and arbiter	Wilma Yeung, Wen Hui Guan
Branch Target predictor	Sonkai Lao
Tracer monitor	Wen Hui Guan
Forwarding Unit	Wilma Yeung
Report write-up	Lin Zhou, Wen Hui Guan

Detailed Strategy:

a. General Design Strategy

Memory System

(1) Instruction Cache and Stream Buffer