EECS 150 - Components and Design Techniques for Digital Systems

Lec 12 - Timing

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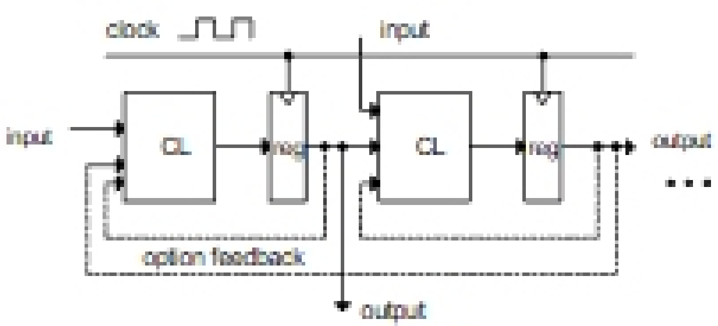
Outline

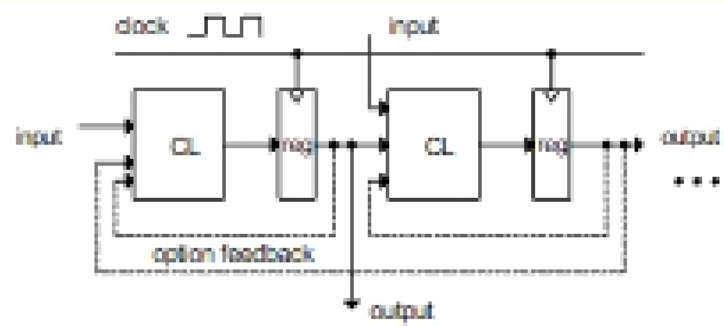
- Performance Limits of Synchronous Systems
- Delay in logic gates
- Delay in wires
- Delay in combinational networks
- Clock Skew
- Delay in flip-flops
- Glitches

Recall: General Model of Synchronous Circuit



- All wires, except clock, may be multiple bits wide.
- Registers (reg)
  - collections of flip-flops
- clock
  - distributed to all flip-flops
  - typical rate?
- Combinational Logic Blocks (CL)
  - no internal state
  - output only a function of inputs
- Particular inputs/outputs are optional
- Optional Feedback

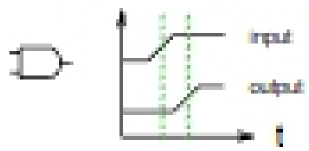
General Model of Synchronous Circuit



- How do we measure performance?
  - operations/sec?
  - cycles/sec?
- What limits the clock rate?
- What happens as we increase the clock rate?

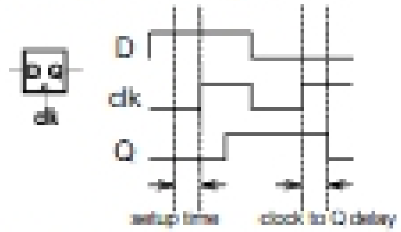
Limitations on Clock Rate

1 Logic Gate Delay



- What are typical delay values?

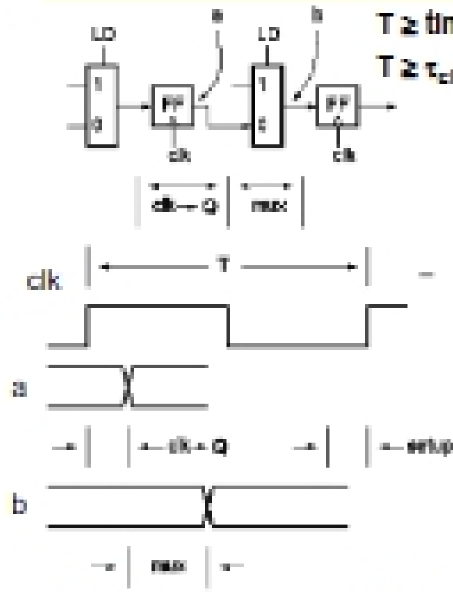
2 Delays in flip-flops



- Both times contribute to limiting the clock period.

- What must happen in one clock cycle for correct operation?
- Assuming perfect clock distribution (all flip-flops see the clock at the same time):
  - All signals must be ready and "setup" before rising edge of clock.

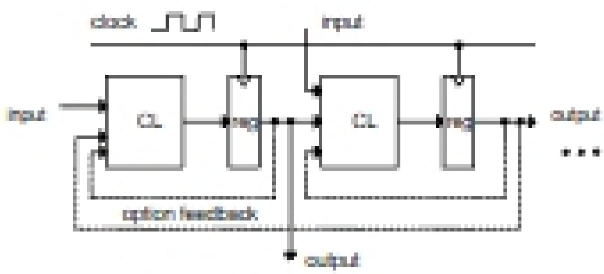
Example: Parallel-Serial Converter



T ≥ time(clk→Q) + time(mux) + time(setup)

$T \geq \tau_{clk \to Q} + \tau_{mux} + \tau_{setup}$

General Model of Synchronous Circuit



- In general, for correct operation:

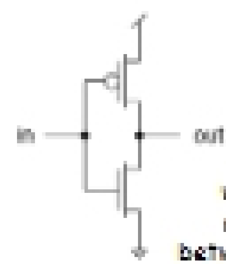
T ≥ time(clk→Q) + time(CL) + time(setup)

$T \geq \tau_{clk \to Q} + \tau_{CL} + \tau_{setup}$ for all paths.

- How do we enumerate *all paths*?
  - Any circuit input or register output to any register input or circuit output.
  - "setup time" for circuit outputs depends on what it connects to
  - "clk-Q time" for circuit inputs depends on from where it comes.

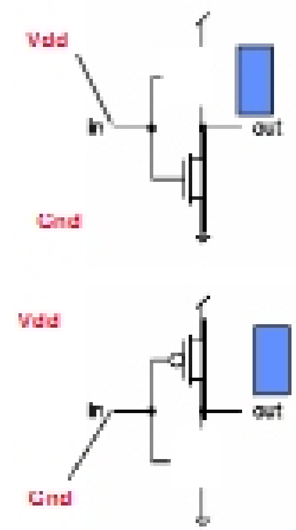
Recall L2: Transistor-level Logic Circuits

- Inverter (NOT gate):



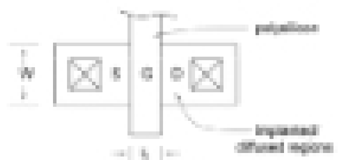
what is the relationship between in and out?

in	out
0 volts	
3 volts	

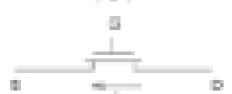


Qualitative Analysis of Logic Delay

- Improved Transistor Model:

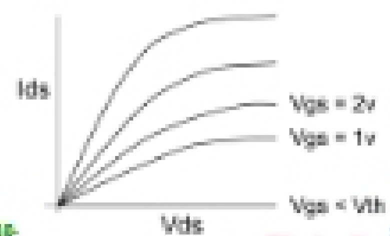


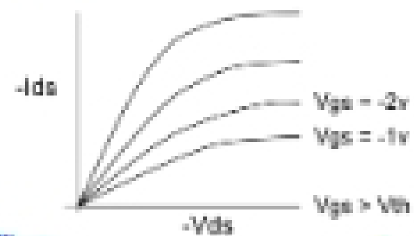
nFET



pFET

- We refer to transistor "strength" as the amount of current that flows for a given Vds and Vgs.
- The strength is linearly proportional to the ratio of W/L
  - Physical property
- Turn it on harder allows more current to flow

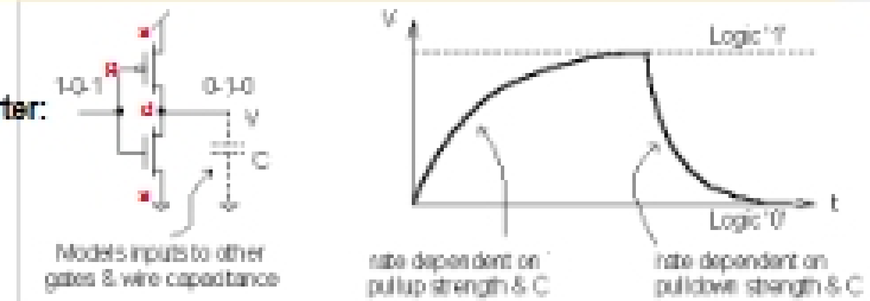




What is the effective resistance?

Gate Switching Behavior

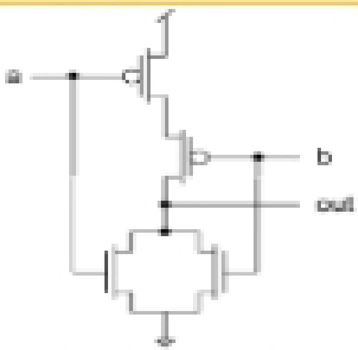
- Inverter:



- NAND gate:

When does it start? How quickly does it switch?

Clarify your understanding



What is the 0 → 1 and 1 → 0 behavior of a NOR gate?

Why do we need pMOS and nMOS devices in a pass gate?

- used for tristate

Delays in a series of gates

- Cascaded gates: