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# CSE 502 Graduate Computer Architecture

## Lec 1-2 - Introduction

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**Slides adapted from David Patterson, UC-Berkeley cs252-s06**

# Outline

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- **Computer Science at a Crossroads**
- **Computer Architecture v. Instruction Set Arch.**
- **How would you like your CSE502?**
- **What Computer Architecture brings to table**
  - Quantitative Principles of Design
  - Technology Performance Trends
  - Careful, Quantitative Comparisons

# Crossroads: Conventional Wisdom in Comp. Arch

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- Old Conventional Wisdom: Power is free, Transistors expensive
  - New Conventional Wisdom: “Power wall” Power expensive, Xtors free (Can put more on chip than can afford to turn on)
  - Old CW: Can increase Instruction Level Parallelism more via compilers, innovation (Out-of-order, speculation, VLIW, ...)
  - New CW: “ILP wall” law of diminishing returns on more HW for ILP
  - Old CW: Multiplies are slow, Memory access is fast
  - New CW: “Memory wall” Memory slow, multiplies fast (200 clock cycles to DRAM memory, 4 clocks for multiply)
  - Old CW: Uniprocessor performance 2X / 1.5 yrs
  - New CW: Power Wall + ILP Wall + Memory Wall = Brick Wall
    - Uniprocessor performance now 2X / 5(?) yrs
- ⇒ Sea change in chip design: multiple “cores” (2X processors per chip / ~ 2 years)
- » Increase on-chip number of simple processors that are power efficient
  - » Simple processor “cores” use less power per useful calculation done