

680XX Hardware Interface

- **Outline**
 - 680XX Family Hardware Interfaces
 - 68000 Hardware Interface
- **Goal**
 - Understand 680XX hardware interfaces
 - Learn how to attach memory, peripherals to CPU
- **Reading**
 - *Microprocessor Systems Design*, Clements, Ch. 4

680XX Family Hardware Interfaces

- **68000**
 - asynchronous interface
 - » request/acknowledge sequencing, no clock
 - 24-bit address, 16-bit data
 - handles bus arbitration
- **68020**
 - asynchronous
 - 32-bit address, 32-bit data
 - dynamic bus sizing
- **68030**
 - 68020 plus synchronous mode
 - burst-mode to fill cache
- **68040**
 - fully synchronous
 - external arbitration

68000 Hardware Interface

- **Figure 4.1 in text**
- **64-pin package**
 - **system support pins**
 - » **power, clock, reset, etc.**
 - **memory and peripheral interface pins**
 - » **data I/O**
 - **special-purpose pins**
 - » **interrupt management and bus arbitration**
 - » **Table 4.1 in textbook**
- **Signal conventions**
 - ***asserted*** - signal is in active state
 - ***negated*** - signal is in inactive state
 - **asterisk suffix - active-low** - active when at electrically low state, i.e. at ground
 - » **example - RESET***