ECE 126 – **Inverter Tutorial: Mixed Signal Simulation: Using Verilog as Input Stimulus**

Created at GWU by Thomas Farmer

Objectives:
- Create a verilog test bench for an inverter
- Use the Cadence configuration hierarchy editor tool

Assumptions:
- Student has a basic familiarity with verilog
- Student is familiar with simulating off the 'extracted view' of a layout

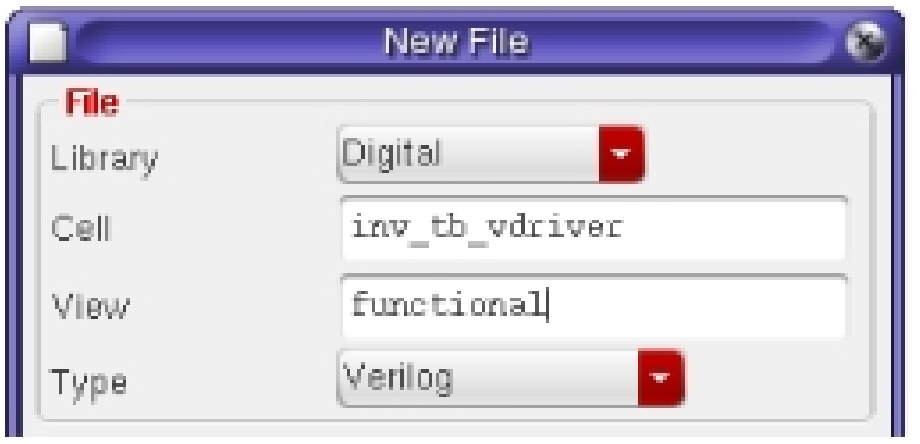
Introduction:
Up to this point you have used "pulses" and "dc sources" in your test benches to test your Cadence schematics and layouts. In this lab you will learn to create and use a verilog 'source' to test your Cadence schematics and layouts. This will enable you to create more complex test-benches for your final project.

LAB SETUP:

1. BEFORE starting cadence, type the following command in a terminal window:

In lab 2, a pulsed waveform was used to provide stimulus for your inverter. In this section, you will create a verilog-driver (very simple verilog code), to replace the pulsed waveform from lab 2.

1. Create a new cell in your Digital Library, called: inv_tb_vdriver

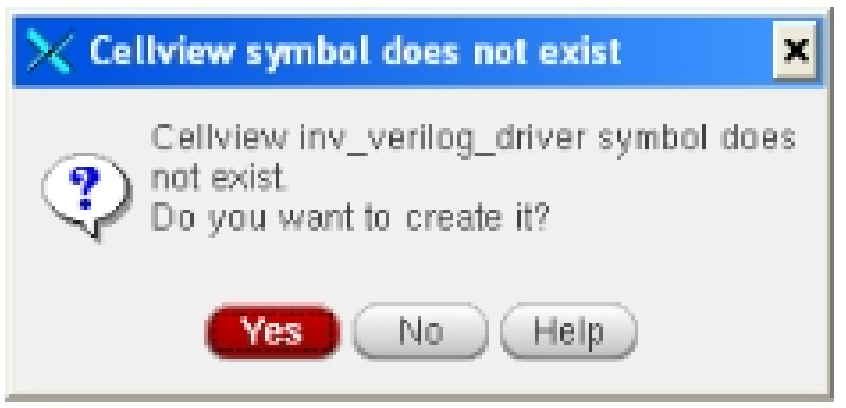


2. Edit the verilog code:

- The "GEDIT" editor should appear
- Replace the skeleton verilog code with the following verilog code (copy & paste this code):

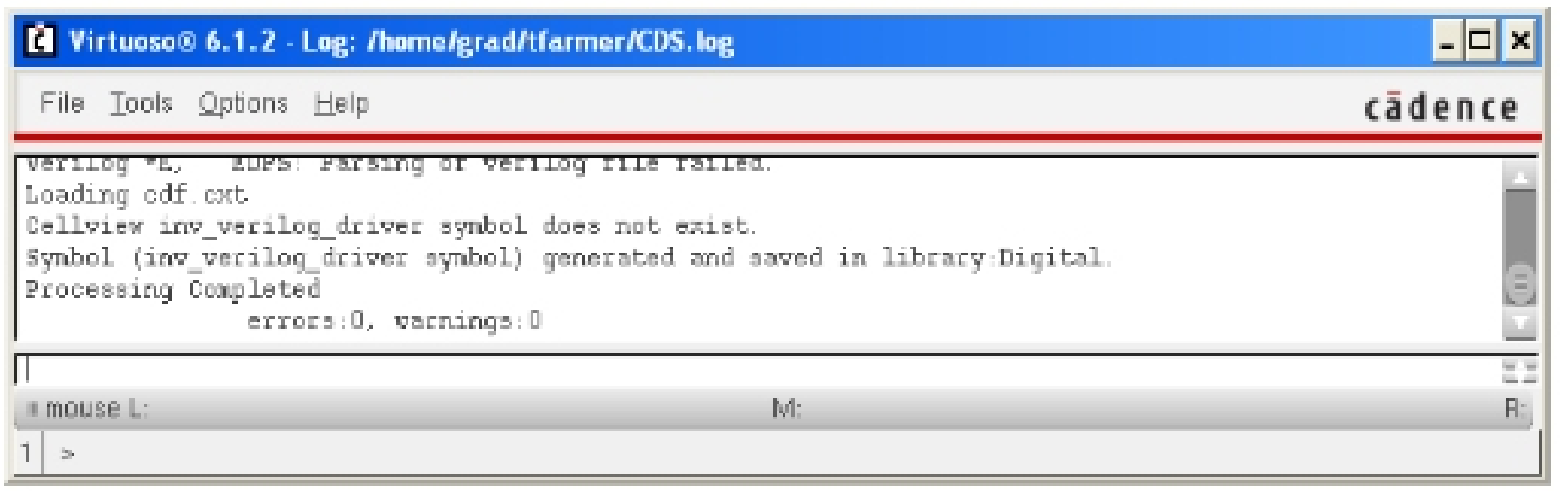
3. *Exit the GEDIT editor, answer SAVE when prompted.*
    - Cadence then compiles the verilog code. Check the CIW and see if there are any errors or warnings. If there are, ensure you copied the code correctly into GEDIT.

4. *When prompted to create a symbol for your verilog code, choose "YES"*



    - Cadence automatically generates a symbol for your verilog code. It will have 1 output line called: test_data as you specified in the code.

5. *Ensure from the CIW, that there are 0 errors and 0 warnings in your verilog driver code:*



    - Now that you have created the verilog-driver, we will instance it in a test bench for our inverter in the next section.