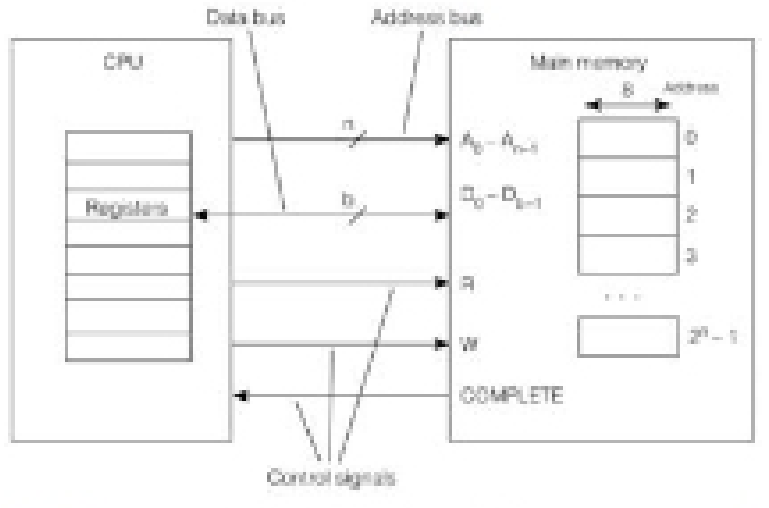
Class 3: Instruction Set Architectures

ISA Components

- Storage cells
  - Registers, memory, etc.
- The Machine Instruction Set
  - Set of possible operations
- The Instruction Format
  - Size and meaning of fields within the instruction

Memory



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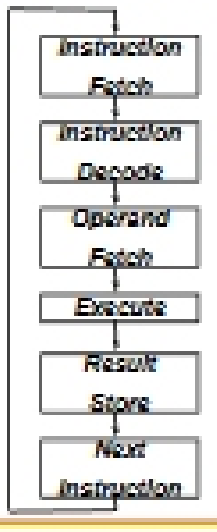
What do instructions need to specify?

- Which operation to perform
  - `add r0, r1, r3  // operation code`
- Where to find the operand or operands
  - `add r0, r1, r3  // source operands`
- Place to store result
  - `add r0, r1, r3  // destination`
- Location of next instruction
  - `add r0, r1, r3`
    `br endloop`

Basic Instruction Cycle



Classes of Instructions

- **Data movement instructions**
  - Load—source is memory and destination is register
  - Store—source is register and destination is memory
- **Arithmetic and logic (ALU) instructions**
  - Add, Sub, Shift, etc.
- **Branch instructions** (control flow instructions)
  - Br Loc, Brz Loc2,—unconditional or conditional branches

Tbl. 2.1 Examples of Data Movement Instructions

Hypothetical Machine Models

Fig. 2.3 The 4-Address Instruction

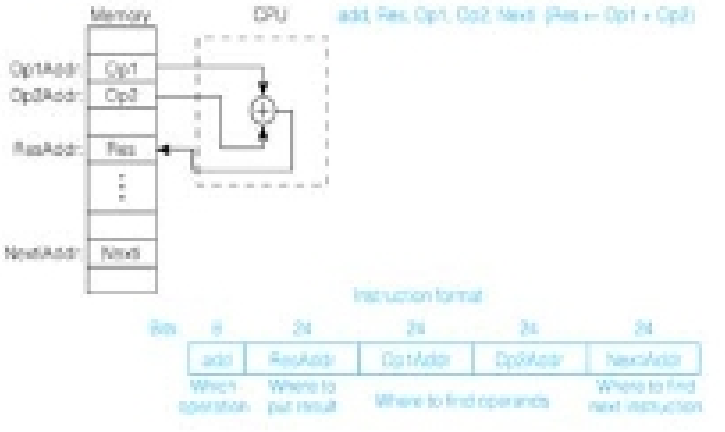


Fig 2.4 The 3 Address Instruction

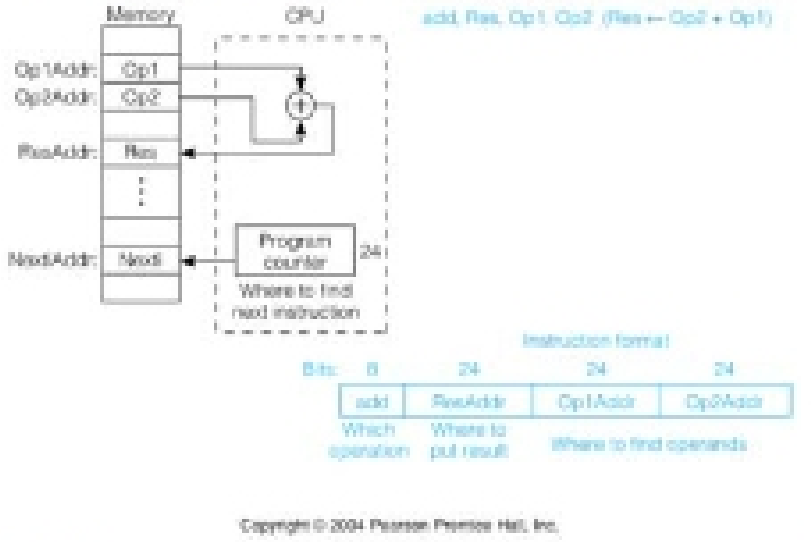


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Fig. 2.5 The 2 Address Instruction

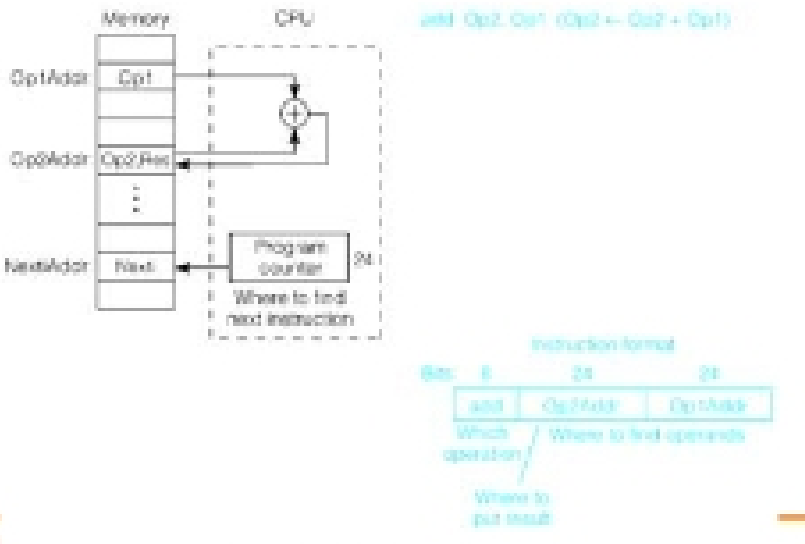

Fig. 2.6 1 Address Instructions

We now need instructions to load and store operands:
LDA OpAddr
STA OpAddr

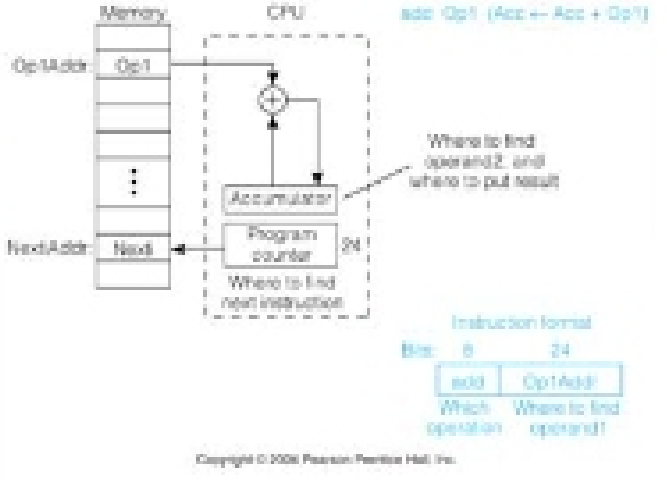

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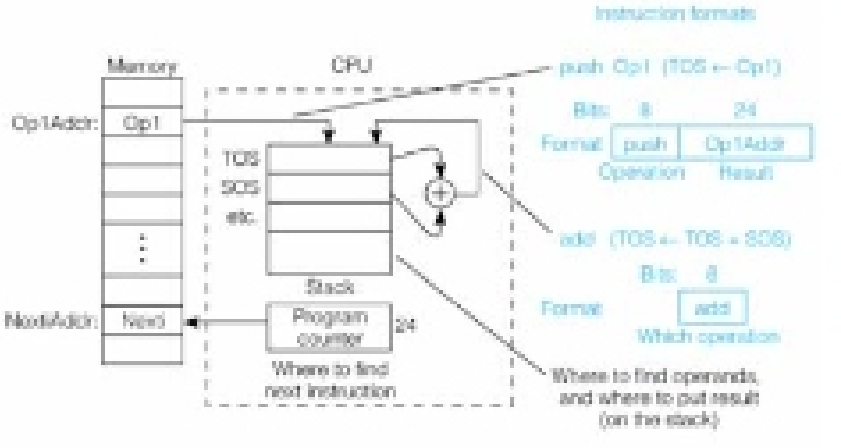
Fig. 2.7 The 0 Address Instruction



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