EE 462: Laboratory Assignment 8
Small Signal Models: The MOSFET Common Source Amplifier

by
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Laboratory # 9 Pre-lab due at lab sessions October 28, 29 and 30.
Lab due at lab sessions November 4, 5, and 6.

I. Instructional Objectives

- Estimate small-signal MOSFET model parameters from measurements
- Analyze circuit using the small-signal transistor model

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2See 6.1, 7.3.3, and 7.4.3 in Horenstein

II. Background

Lab 7 established the quiescent operating point of (biased) a common source amplifier employing an N-channel MOSFET. The common source amplifier is general-purpose amplifier with a good negative voltage gain, but poor high frequency characteristics. The N-channel MOSFET based common source amplifier may be used as a voltage amplifier by connecting an input signal to the gate of the transistor, and connecting a load to the drain. To ensure the input signal and output load do not upset the amplifier's bias, these connections are capacitively coupled. This means a capacitor is connected in series with the signal source and load, providing an open circuit during DC operation in order to prevent the source and load from changing the circuit's quiescent operating point. These capacitor values are chosen so that they behave as an effective short-circuit for the AC signal components and thus that they do not significantly effect the AC signal losses. The circuit used for this lab is shown in Fig. 1, and the small-signal model of the MOSFET used in this circuit is shown in Fig. 2, where r_d and r_{in} are the MOSFET's output resistance and input resistances, respectively.

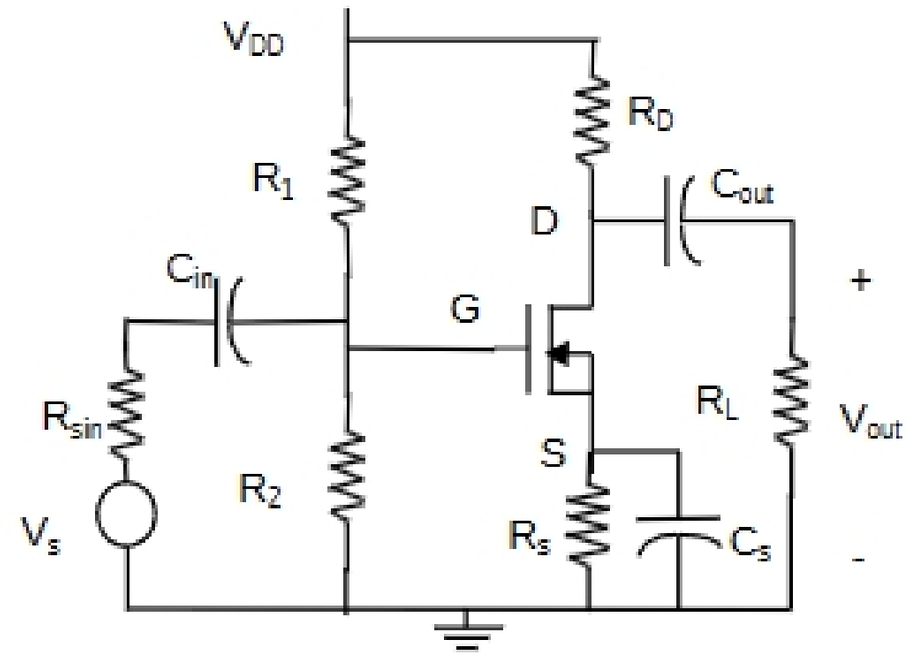

Fig. 1. N-channel MOSFET common source amplifier

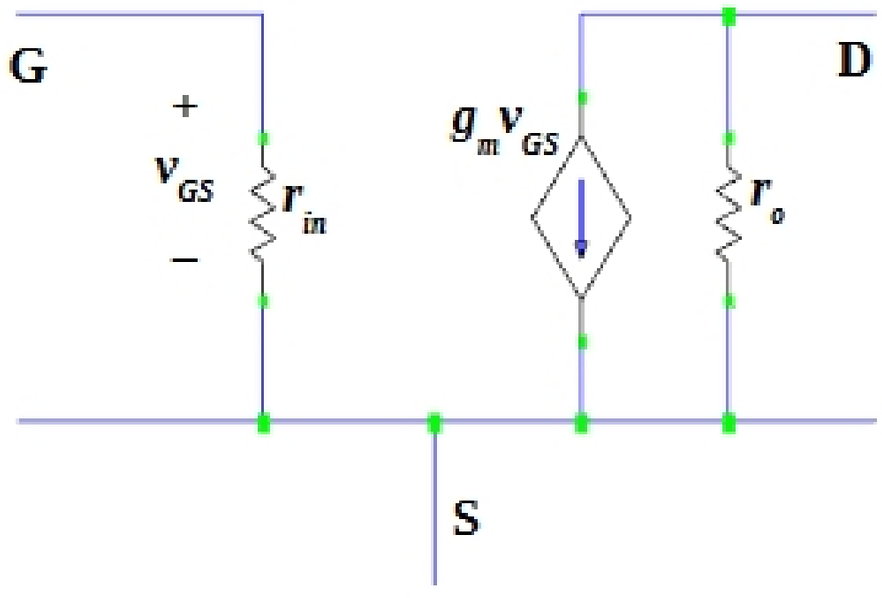

Fig. 2. Small-signal MOSFET model

The parameters for the small signal model are given by:

$$g_m = \hat{i}_D / \hat{v}_{GS} = \left.\frac{\partial I_D(V_{GS})}{\partial V_{GS}}\right|_{v_{gs}=V_{gsQ}} = 2K(V_{GSQ} - V_{tr}) = 2\sqrt{K \cdot I_{DQ}}$$

(1)

where K is the notation used in Horenstein, or

$$g_m = \hat{i}_D / \hat{v}_{GS} = \left.\frac{\partial I_D(V_{GS})}{\partial V_{GS}}\right|_{v_{gs}=V_{gsQ}} = Kp(V_{GSQ} - V_{tr}) = \sqrt{2Kp \cdot I_{DQ}} \qquad (2)$$

where Kp is the notation used in SPICE. Let g_m denote the MOSFET's transconductance. Two other circuits useful for this lab in measuring the total amplifier's input and output resistances are given in Figs. 3 and 4 below.

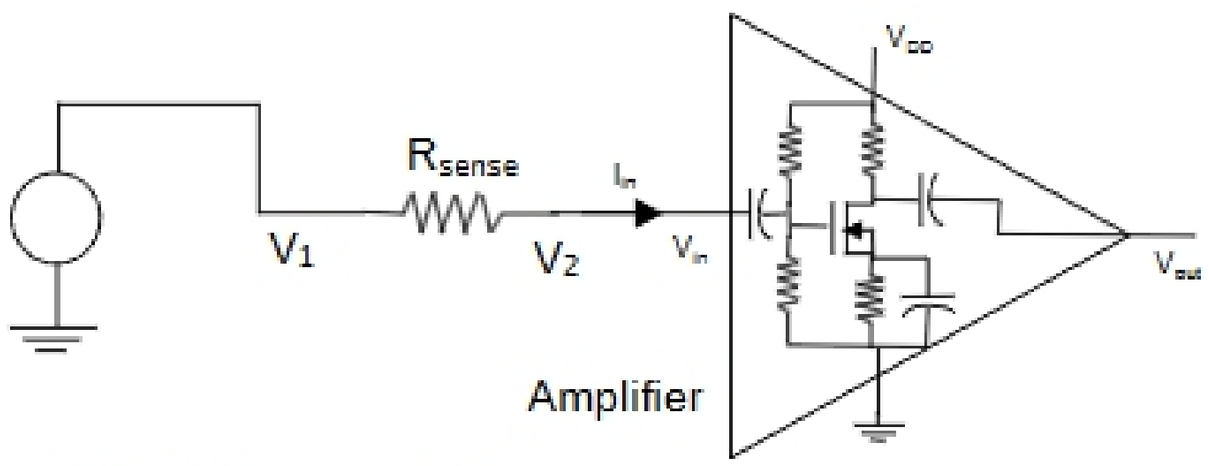

Fig. 3 Circuit for measuring R_{in}.

Relationship for input resistance in terms of measured quantities from the circuit in Fig. 3:

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{inpp}}{I_{inpp}} = \frac{V_{inp}}{I_{inp}} = \frac{V_{inrms}}{I_{inrms}} = \frac{V_2}{\frac{V_1 - V_2}{R_{sense}}} = \frac{V_2 R_{sense}}{V_1 - V_2}$$

(4)

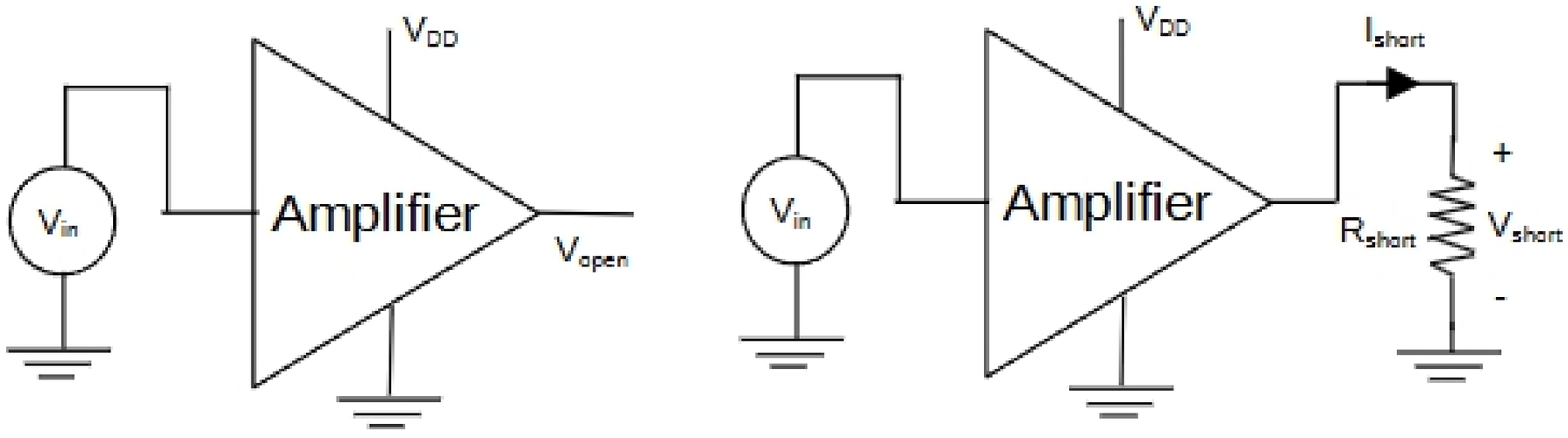

Fig. 4 Circuit for measuring R_{out}.

Relationship for input resistance in terms of measured quantities from the circuit in Fig. 4:

$$R_{out} = R_{th} = \frac{V_{open}}{I_{short}} = \frac{V_{openpp}}{I_{shortpp}} = \frac{V_{openp}}{I_{shortp}} = \frac{V_{openrms}}{I_{shortrms}} = \frac{V_{open}}{\frac{V_{short}}{R_{short}}} = \frac{V_{open} R_{short}}{V_{short}} \quad (4)$$

Note that two separate tests are required to measure the input and output resistances.

III. Pre-Laboratory Exercise

For the pre-lab assignments assume r_d and r_{in} to be infinite. In addition, assume that R_{sin} = 1 k□, R_D = 1 k□, R_s = 100 □, R_L = 1k□, $K = Kp / 2$ =0.1125 A/V^2, V_{tr} = 2.1V, (or you can use the values you measured in the previous labs) I_{R1} = I_{R2} = 1.475mA, and V_{DD} = 15 V. In general the capacitor values should be large to minimize the AC voltage drops for the frequencies considered. Value of C_s will be computed in pre-lab and C_{in} and C_{out} can be set to the value of C_s or greater.

1. Draw the DC model of the circuit. Derive and draw the DC load line equation for the circuit.
2. Set the operating point $V_{DSQ} = V_{DD} / 2$ which is approximately the intersection of the midpoint of the load line and the characteristic curves for the NMOSFET. You can draw or plot these curves knowing K or Kp as done in a previous lab. Since most of the operation will be in the saturation region, the following relationship is all that is needed to relate the gate voltage to the drain current:

$$I_D = K(V_{GS} - V_{tr})^2 = \frac{Kp}{2}(V_{GS} - V_{tr})^2 \text{ for } V_{DS} > V_{GS} - V_{tr} \quad (3)$$

3. Find the values of R_1 and R_2, to set the operating point (I_{DQ}, V_{DSQ}).
4. Draw the AC or incremental model of the circuit.
5. Using the AC or incremental model, determine the small signal voltage gain ($\hat{v}_{out} / \hat{v}_{in}$) and current gain ($\hat{i}_{out} / \hat{i}_{in}$) of the circuit for C_S = 0. For these calculations assume R_{sin} is zero and R_L is infinite. Repeat the voltage gain calculation with the given values of R_{sin} and R_L (1 k□).
6. Determine the small signal voltage ($\hat{v}_{out} / \hat{v}_{in}$) and current gain ($\hat{i}_{out} / \hat{i}_{in}$) of the circuit for C_S so large that it shorts out R_S. For this calculation you may again assume R_{sin} is zero and R_L is infinite. Repeat the voltage gain calculation with the given values of R_{sin} and R_L.