EECS150 - Digital Design

Lecture 12 - Combinational Logic & Arithmetic Circuits Part 2

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Carry Look-ahead Adders

- In general, for n-bit addition best we can achieve is

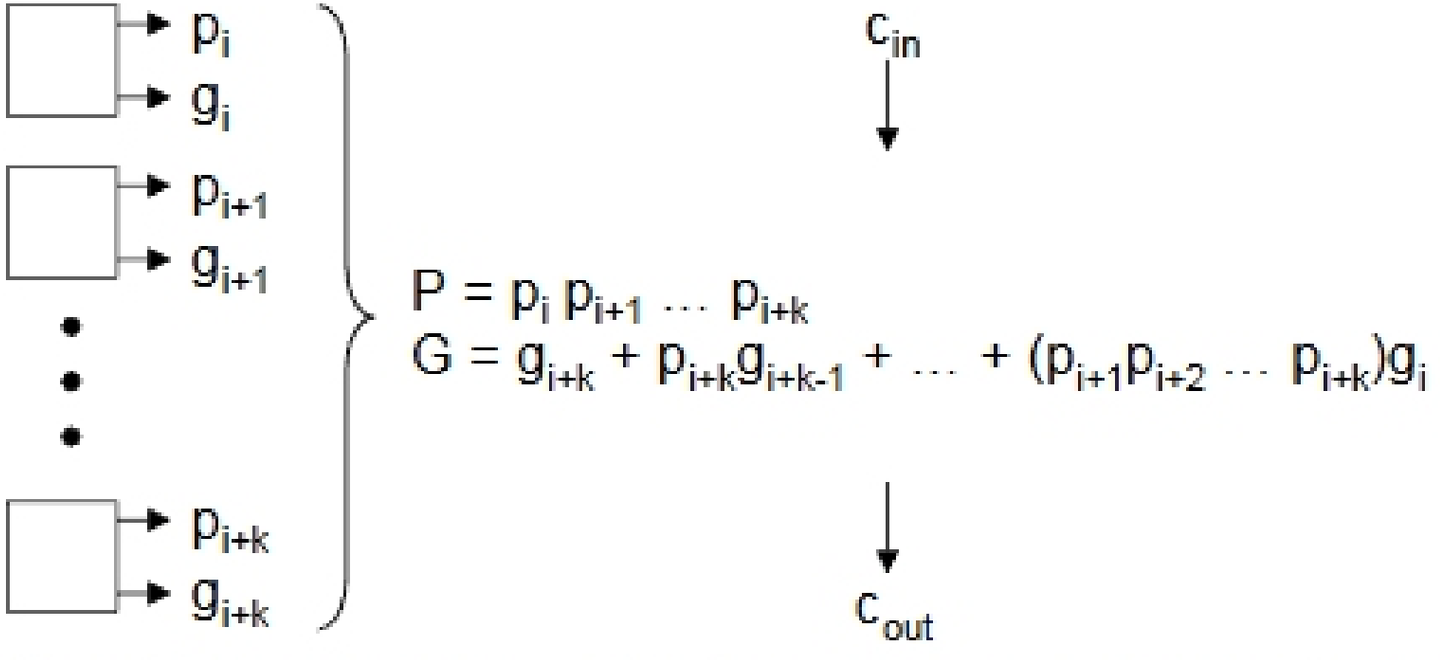
  delay α log(n)
- How do we arrange this? (think trees)
- First, reformulate basic adder stage:

a b c_i	c_{i+1}	s	
0 0 0	0	0	carry "kill"
0 0 1	0	1	$k_i = a_i' \, b_i'$
0 1 0	0	1	
0 1 1	1	0	carry "propagate"
1 0 0	0	1	$p_i = a_i \oplus b_i$
1 0 1	1	0	
1 1 0	1	0	carry "generate"
1 1 1	1	1	$g_i = a_i \, b_i$

$$c_{i+1} = g_i + p_i c_i$$
$$s_i = p_i \oplus c_i$$

Carry Look-ahead Adders

- "Group" propagate and generate signals:



- P true if the group as a whole propagates a carry to c_{out}
- G true if the group as a whole generates a carry

- Group P and G can be generated hierarchically.

$$C_{out} = G + PC_{in}$$