CS 152 Computer Architecture and Engineering

Lecture 15 - Advanced Superscalars

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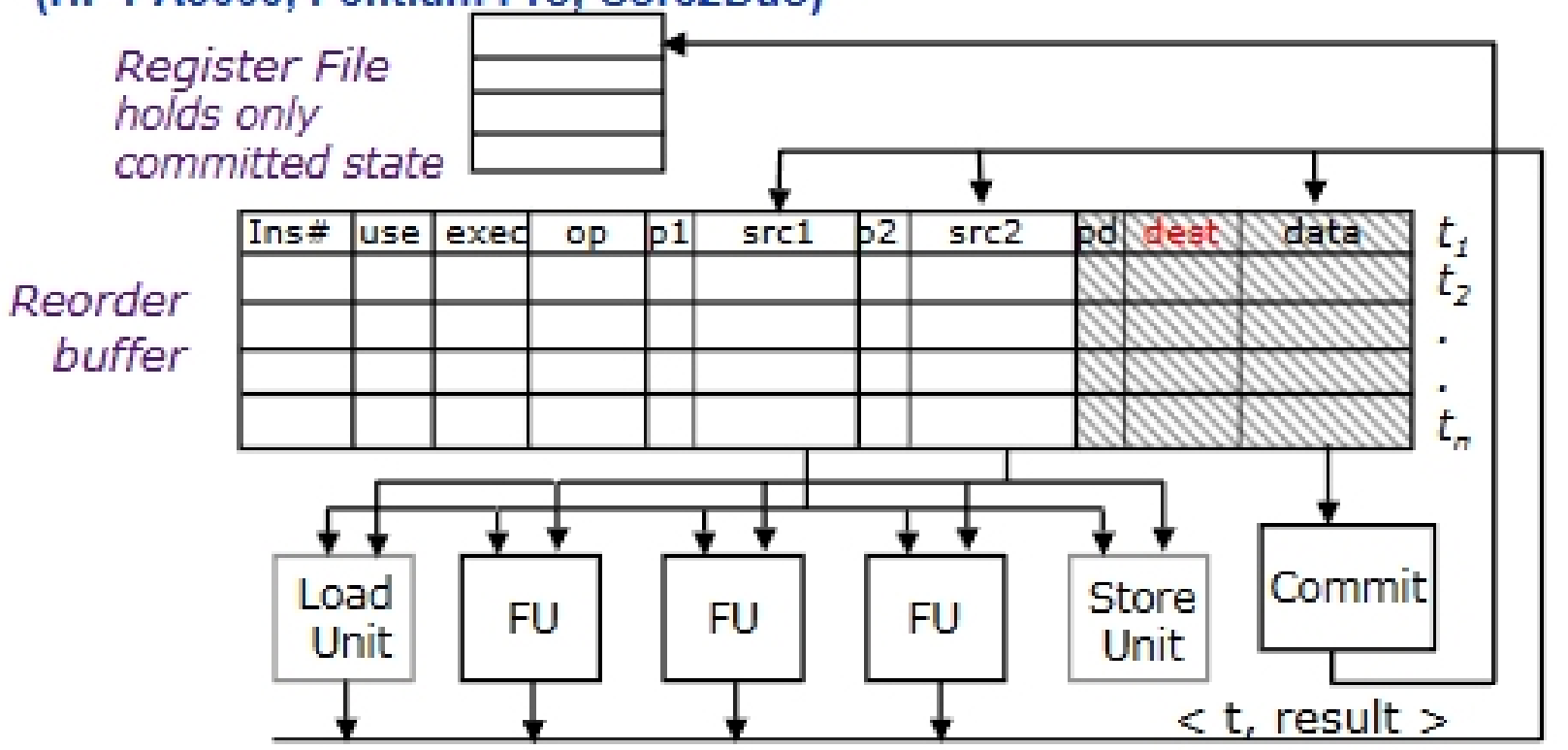
Last time in Lecture 14

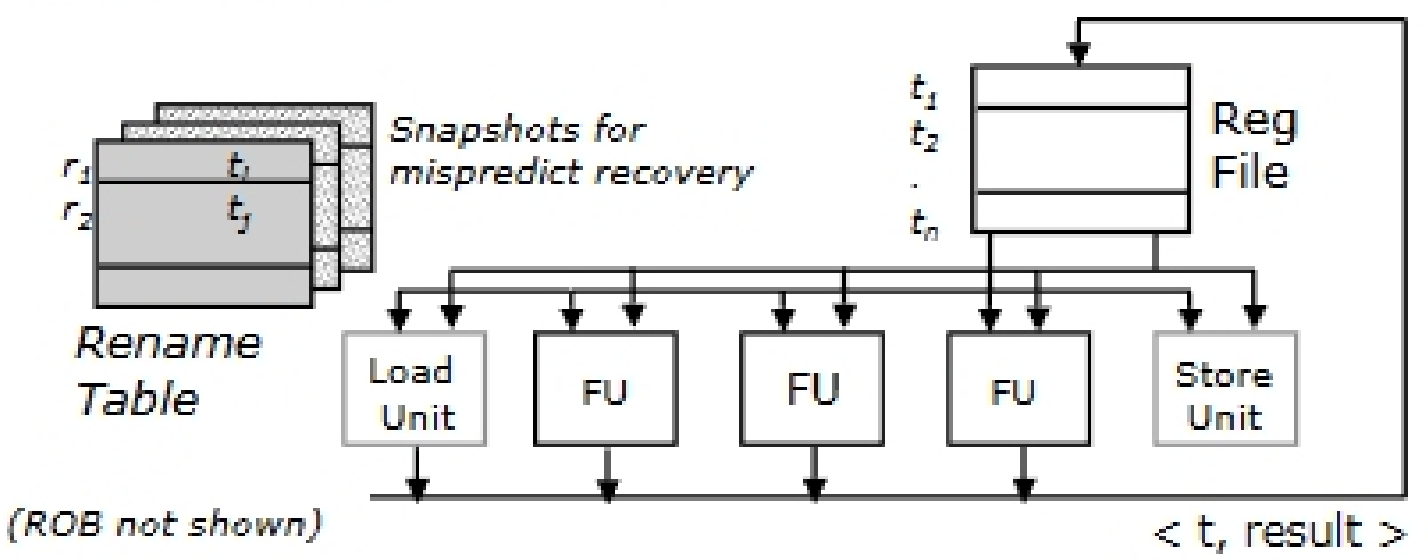
- Control hazards are serious impediment to superscalar performance
- Dynamic branch predictors can be quite accurate (>95%) and avoid most control hazards
- Branch History Tables (BHTs) just predict direction (later in pipeline)
  - Just need a few bits per entry (2 bits gives hysteresis)
  - Need to decode instruction bits to determine whether this is a branch and what the target address is
- Branch Target Buffer (BTB) predicts whether a branch, and target address
  - Needs PC tag, predicted Next-PC, and direction
  - Just needs PC of instruction to predict target of branch (if any)
- Return address stack: special form of BTB used to predict subroutine return addresses

"Data in ROB" Design
(HP PA8000, Pentium Pro, Core2Duo)



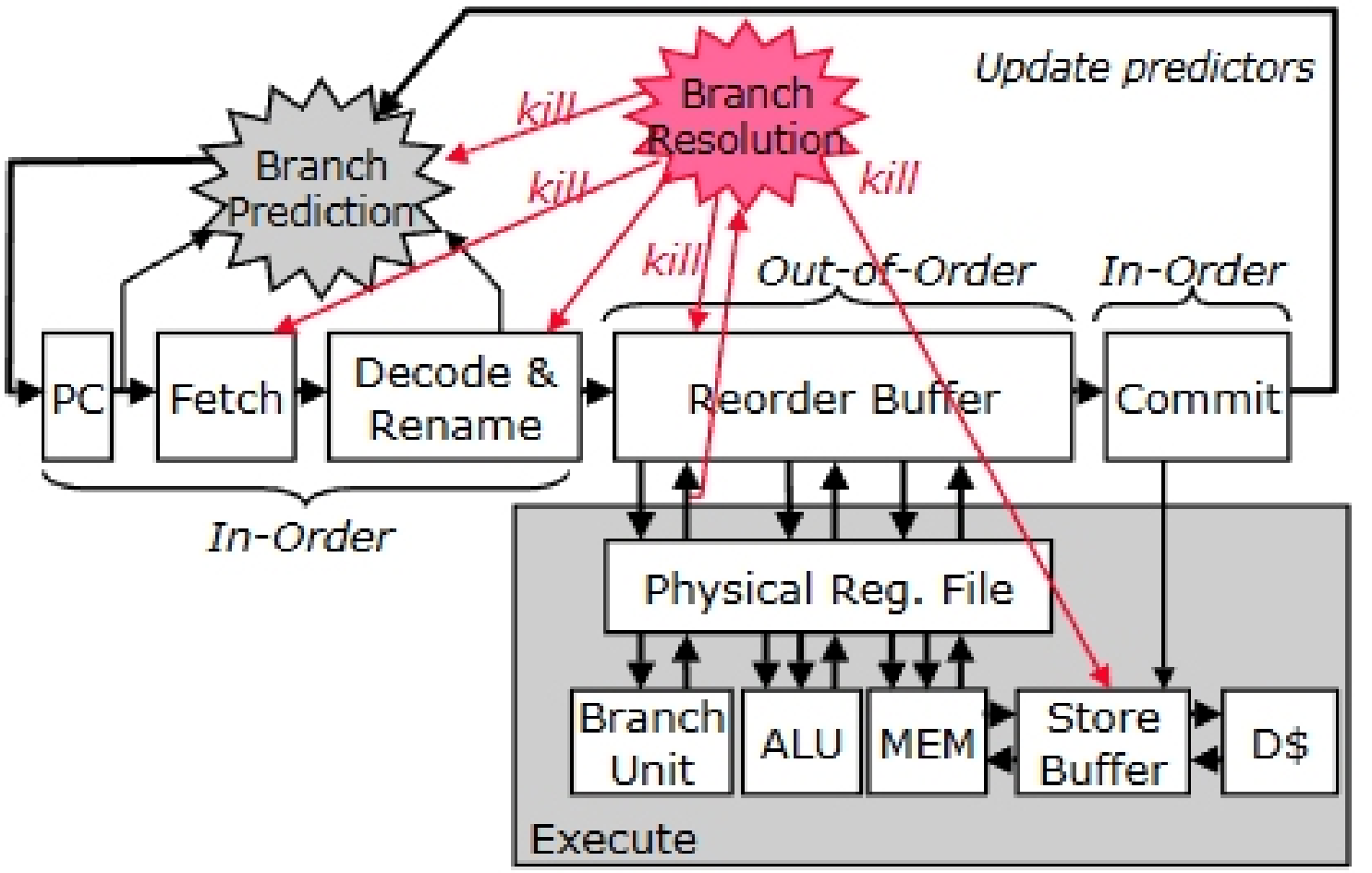
- On dispatch into ROB, ready sources can be in regfile or in ROB dest (copied into src1/src2 if ready before dispatch)
- On completion, write to dest field and broadcast to src fields.
- On issue, read from ROB src fields

Unified Physical Register File
(MIPS R10K, Alpha 21264, Pentium 4)



- One regfile for both *committed* and *speculative* values (no data in ROB)
- During decode, instruction result allocated new physical register, source regs translated to physical regs through rename table
- Instruction reads data from regfile at start of execute (not in decode)
- Write-back updates reg. busy bits on instructions in ROB (assoc. search)
- Snapshots of rename table taken at every branch to recover mispredicts
- On exception, renaming undone in reverse order of issue *(MIPS R10000)*

Pipeline Design with Physical Regfile



Lifetime of Physical Registers

- Physical regfile holds committed and speculative values
- Physical registers decoupled from ROB entries *(no data in ROB)*

ld r1, (r3)		ld P1, (P*x*)
add r3, r1, #4		add P2, P1, #4
sub r6, r7, r9		sub P3, P*y*, P*z*
add r3, r3, r6	*Rename*	add P4, P2, P3
ld r6, (r1)		ld P5, (P1)
add r6, r6, r3		add P6, P5, P4
st r6, (r1)		st P6, (P1)
ld r6, (r11)		ld P7, (P*w*)

When can we reuse a physical register?