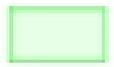
CMOS Layout

- IC design procedure:
  - system specifications
  - circuit design
  - ***layout***
  - ***post-layout extraction and simulation***
  - IC fabrication
  - testing

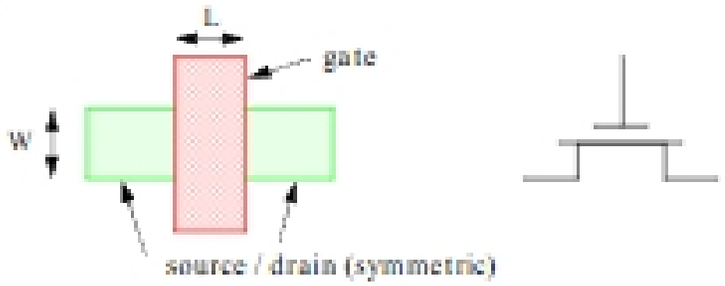
- Layout considerations:
  - mask layers
  - devices
  - electrical connectivity (interconnect)
  - layout (design) rules

Mask Layers

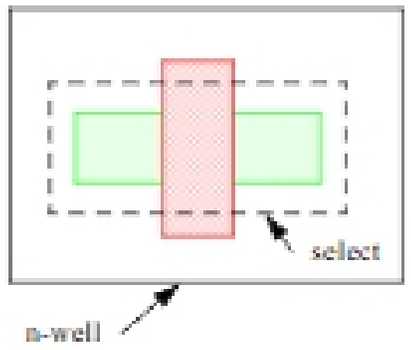
Layer	Representation	Color Convention (EECS 105)
n-well		purple
active		green
select (p^+)		brown
polysilicon		red
metal		blue
contact		black

MOSFET Layout

- *polysilicon* crossing *active* results in an NMOS device:

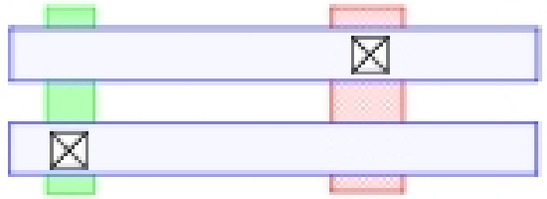


- PMOS devices are placed in *n-wells*:



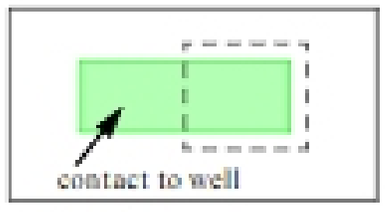
Electrical Connectivity

- *active*, *polysilicon*, and *metal* can be used for interconnects (wires)
- *metal* has much lower resistivity than either *active* or *polysilicon*
- *metal* is separated from *active* or *polysilicon* by an (insulating) oxide; a *contact* is needed for electrical connections between these layers



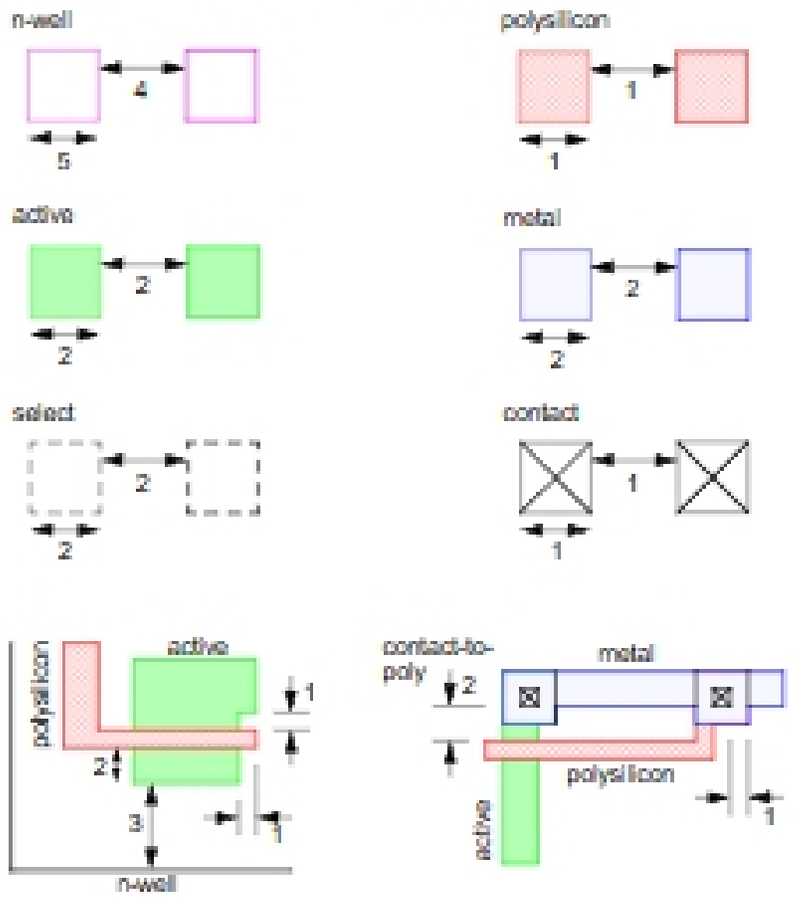
- *active* and *polysilicon* cannot be connected directly (without *metal*)
- use p-doped *active* (*select* mask) as contact to the bulk

  use n-doped *active* (no *select* mask) as a contact to *n-wells*

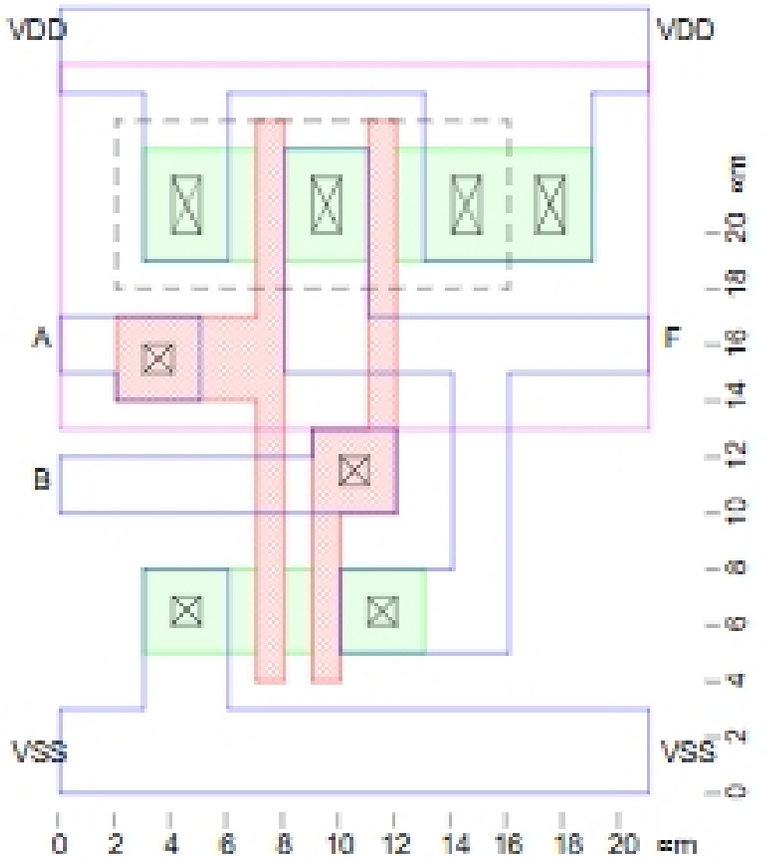


Layout Rules (EECS 105 Technology)

minimum dimensions and separations (in mm, not to scale):



Layout Example



EE 105 Fall 1998
Lecture 12