# EECS150 - Digital Design

## Lecture 26 – Error Correction Codes, Linear Feedback Shift Registers (LFSRs)

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# Outline

- Error detection using parity
- Hamming code for error detection/correction
- Linear Feedback Shift Registers
  - Theory and practice

# Error Correction Codes (ECC)

- Memory systems generate errors (accidentally fliped-bits)
  - DRAMs store very little charge per bit
  - "Soft" errors occur occasionally when cells are struck by alpha particles or other environmental upsets.
  - Less frequently, "hard" errors can occur when chips permanently fail.
- Where "perfect" memory is required
  - servers, spacecraft/military computers, …
- Memories are protected against failures with ECCs
- Extra bits are added to each data-word
  - extra bits are used to detect and/or correct faults in the memory system
  - in general, each possible data word value is mapped to a unique "code word". A fault changes a valid code word to an invalid one - which can be detected.